

**Statement of Work (SOW)  
For the Development of  
The High Performance Space Computing (HPSC) Processor**

**10/08/2015**

**1.0 Introduction/Background:**

NASA and USAF require High Performance Space Computing (HPSC) for multiple mission applications associated with both robotic and human space exploration. Traditionally, spacecraft onboard computing systems are single processor systems based on existing commercial or military computers that are radiation hardened. The systems are implemented and operated at maximum required mission performance point, where the term “performance point” includes throughput, fault tolerance and power levels. As NASA and USAF consider advanced missions that require both an increase in throughput and wider variations in these operating points, the development of a new processor is needed. This processor, termed “the chiplet” herein, is needed to provide orders of magnitude improvement in performance and performance-to-power ratio as well as the ability to dynamically set the power-throughput-fault tolerance operating point. The purpose of this draft Statement of Work (SOW) is to solicit information for the development of this new processor.

This project will consist of a preliminary design phase culminating in a Preliminary Design Review (PDR), a detailed design phase culminating in a Critical Design Review (CDR), a fabrication phase, and a test and characterization phase. The project duration is baselined at four years.

This project will deliver: chiplet software emulator and FPGA implementations, prototype processor “chiplets” packaged and functionally tested at ambient temperature, chiplet evaluation boards and system software as defined below.

**1.1 Background**

NASA has conducted a High Performance Space Computing (HPSC) study defining future spacecraft onboard computing needs. Several HPSC use cases were identified, broadly addressing both human spaceflight missions and robotic science. As shown below, these were categorized into (a) vision-based algorithms with real-time requirements, (b) model-based reasoning techniques for autonomy, and (c) high rate instrument data processing.

Computation Category	Mission Need	Objective of Computation	Flight Architecture Attribute
<b>Vision-based Algorithms with Real-Time Requirements</b>	<ul style="list-style-type: none"> <li>• Terrain Relative Navigation (TRN)</li> <li>• Hazard Avoidance</li> <li>• Entry, Descent &amp; Landing (EDL)</li> <li>• Pinpoint Landing</li> </ul>	<ul style="list-style-type: none"> <li>• Conduct safe proximity operations around primitive bodies</li> <li>• Land safely and accurately</li> <li>• Achieve robust results within available timeframe as input to control decisions</li> </ul>	<ul style="list-style-type: none"> <li>• Severe fault tolerance and real-time requirements</li> <li>• Fail-operational</li> <li>• High peak power needs</li> </ul>
<b>Model-Based Reasoning Techniques for Autonomy</b>	<ul style="list-style-type: none"> <li>• Mission planning, scheduling &amp; resource management</li> <li>• Fault management in uncertain environments</li> </ul>	<ul style="list-style-type: none"> <li>• Contingency planning to mitigate execution failures</li> <li>• Detect, diagnose and recover from faults</li> </ul>	<ul style="list-style-type: none"> <li>• High computational complexity</li> <li>• Graceful degradation</li> <li>• Memory usage (data movement) impacts energy management</li> </ul>
<b>High Rate Instrument Data Processing</b>	<ul style="list-style-type: none"> <li>• High resolution sensors, e.g., SAR, Hyper-spectral</li> </ul>	<ul style="list-style-type: none"> <li>• Downlink images and products rather than raw data</li> <li>• Opportunistic science</li> </ul>	<ul style="list-style-type: none"> <li>• Distributed, dedicated processors at sensors</li> <li>• Less stringent fault tolerance</li> </ul>

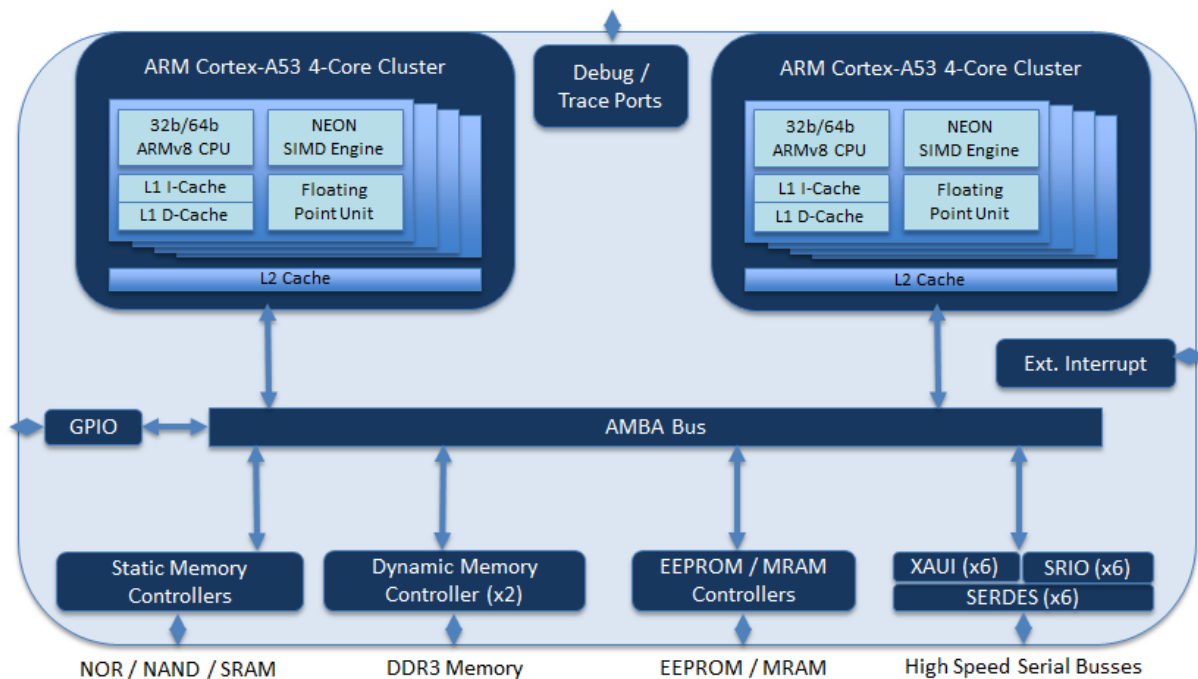
These applications were classified into a set of “eigen applications”, each of which defines the processing requirements and characteristics of a subset of the mission applications. Based on these requirements and other key performance parameters (including power/energy management, fault tolerance, programmability, interoperability, evolvability/extensibility, and cost), candidate computing architectures were evaluated. This evaluation established that a radiation-hardened, general purpose multi-core processor is best suited to address NASA’s future onboard computing needs.

Collaborative discussions with AFRL determined that many of NASA’s future onboard computing needs have commonality with AFRL’s future needs, and that a radiation-hardened, general purpose multi-core processor of the kind envisioned by NASA would also be relevant to AFRL. Based on these shared interests, NASA partnered with AFRL on a Next Generation Space Processor (NGSP) study. This study, led by AFRL, engaged with industry to assess, in greater detail, AFRL’s requirements, compare AFRL’s requirements with NASA’s previously defined detailed requirements, develop processor architectures that would satisfy the superset of NASA/AFRL requirements and evaluate these architectures against a set of government provided benchmarks.

The NGSP study provided the government valuable guidance regarding the optimal architecture for a future spaceflight processing device:

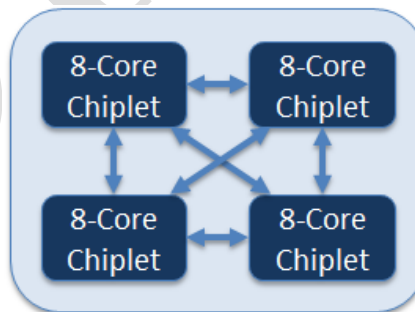
1. The use of COTS IP (specifically ARM based IP) provides optimal power-to-performance, extensibility, evolvability, software availability, ease of use, and cost.
2. The use of Radiation Hard By Design (RHBD) standard cell libraries provides required radiation tolerance.
3. The augmentation of RHBD with higher level fault tolerance techniques improves reliability.
4. The use of the ARM A53 processor with its internal NEON SIMD is sufficient for most near term applications.
5. Heterogeneous multi-core architectures using multiple processor core types are not optimal.
6. Architectural flexibility such as the ability to turn on/off cache coherency and use of L3 cache, as well as the ability to dynamically depower unused cores of all sorts, including memory and I/O interfaces, is useful to enable setting of optimal power:performance:fault tolerance operating point.

Based on these findings, the government team devised the HPSC “chiplet” concept that (a) meets NASA’s future onboard computing needs, and (b) can be developed within the available funding profile. The chiplet concept leverages the COTS ARM A53 IP along with other COTS peripheral IP, and can meet NASA’s performance, power, and radiation tolerance needs when implemented via existing RHBD technology. The chiplet includes multiple Serial RapidIO (SRIO) for high bandwidth communication, and multiple interfaces to high speed off-chip memory.



## 1.2 System Context

The chiplet as specified here provides the performance to satisfy the majority of NASA onboard processing applications as a discrete packaged part. It will also provide extensibility (via SRIIO) to allow the most demanding applications to be satisfied with “multiple-chiplet” systems, implemented either on a multi-chip module (MCM) or on a printed wiring board with multiple discrete chiplets. Multiple-chiplet systems can satisfy needs for requirements for increased processing bandwidth, or by needs for increased fault tolerance (i.e. multiple chiplets as separate fault containment regions).



The SRIIO interface also allows extensibility to other SRIIO-enabled processing devices such as FPGAs, GPUs, and in the future to other ASICs serving as application specific coprocessors.

Viewed as an individual chiplet or as a system of multiple chiplets, a key requirement for HPSC is the flexibility to dynamically trade between processing throughput, power consumption, and fault tolerance to meet varying demands and priorities across multiple candidate missions and within the profile of each mission.

The mission applications for the HPSC chiplet range from human rated spacecraft, habitats, and vehicles to robotic science and exploration platforms, to military surveillance and weapons systems. System applications range from small cubesats to large flagship class missions, and can include:

1. Command & Data Handling, Guidance Navigation & Control, Communications (e.g. Software Defined Radio)
2. Human assist, Data representation, Cloud computing
3. High rate, real time sensor data processing
4. Autonomy, Science processing

In many of these applications the HPSC chiplet (or multiple chiplets) would be implemented within a dedicated spaceflight computer box. Alternatively, the chiplet(s) may be embedded within a science instrument or spaceflight subsystem. The criticality of these applications can range from low criticality science data processing to high criticality human rated applications employing ARINC-653 time space partitioning.

The software infrastructure for the HPSC chiplet will support both symmetric and asymmetric processing, and support both real-time operating systems and Unix/Linux based parallel processing. The software infrastructure will also support hierarchical fault tolerance, ranging from single chiplet small mission to multi-chiplet highly redundant human missions. This software infrastructure is a contract deliverable (detailed below).

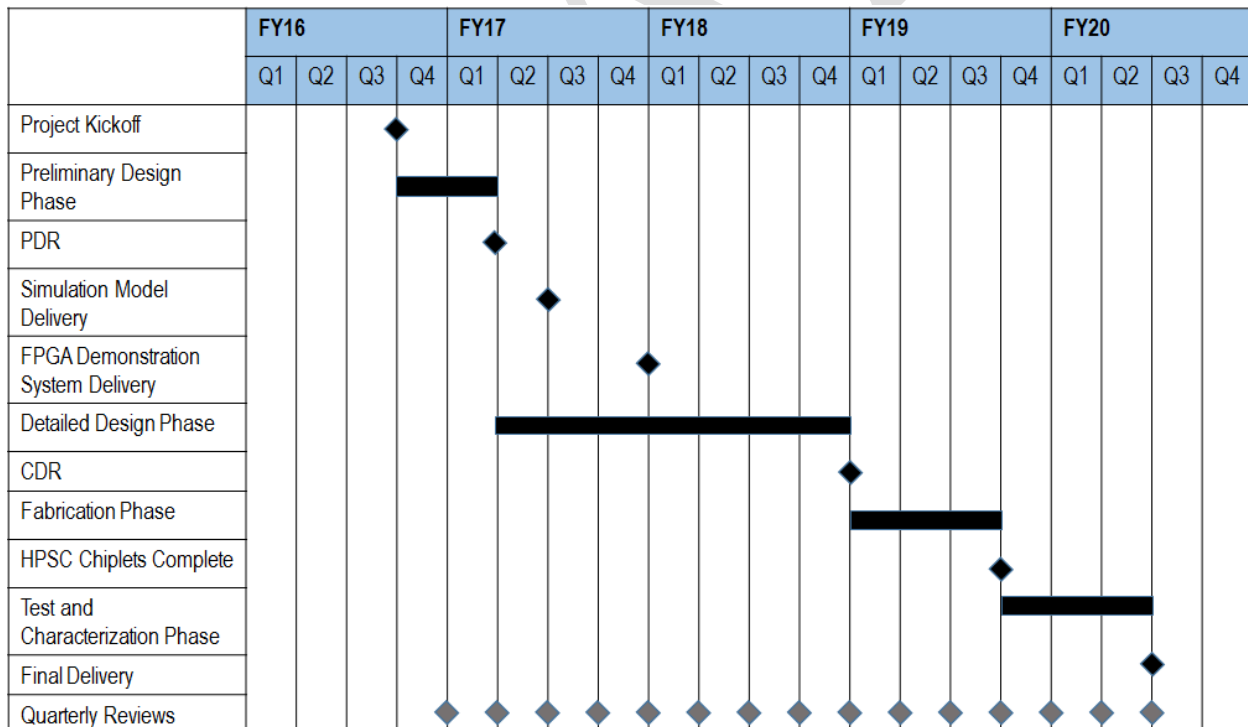
The HPSC chiplet will provide increased processing bandwidth, power efficiency, and fault tolerance for onboard processing applications. However, these advantages could come at the cost of increased hardware and software complexity. As software development and verification is a major cost driver for missions, this increased complexity has the potential to significantly increase cost for future NASA missions. To address this risk, NASA will separately develop **(i.e. not part of this contract)** middleware software providing machine management for multicore processing devices. This middleware software layer shall reside between the application layer and the operating system to provide intelligent resource, fault, and power management. By providing these functions, application software can be largely agnostic to underlying hardware, thereby reducing cost and complexity. During the preliminary design phases of the HPSC chiplet development, interaction with the middleware developers will be needed to ensure that the hardware interfaces enabling this resource management are well understood. Details of the interfaces between middleware and hardware and system software will be jointly defined by the government and vendor prior to PDR.

## 2.0 Scope of Work

The HPSC project is an effort to design and deliver radiation hardened chiplet devices and the evaluation hardware and software to test the full functionality of the chiplets.

The chiplet design will conform to the architecture in Figure 1 and be capable of providing up to 15GOPS for 5-7W, depending on memory and I/O configuration. The chiplets shall be radiation hardened, per the requirements below, in order to ensure correct operation in natural and strategic space environments. The design and/or development of the chiplet shall include a strategy to provide assured integrity (absence of malicious functions/ alterations). The integrity assurance strategy will be reviewed and approved by the Government, which accomplished through the design process flow, the fabrication process, the after fabrication verification process, or a combination of elements.

The project will consist of a preliminary design phase culminating in a Preliminary Design Review (PDR), a detailed design phase culminating in a Critical Design Review (CDR), a fabrication phase, and a test and characterization phase. The project duration is baselined at four years. The chart below shows the project baseline schedule and milestones.



### **3.0 Applicable Documents/Background:**

The following is a list of appropriate specifications, standards and other documents that are applicable to the effort to be performed:

- I/O specifications:
  - o SRIO 3.1
  - o Ethernet IEEE 802.3 10/100
  - o XAUI IEEE 802.3ae
- ARM Documents – <http://www.arm.com/products/index.php>

### **4.0 Description of Work to be performed:**

The following is a description of work to be performed under the contract:

#### **4.1 Monthly Project Status Meetings**

- The Contractor shall participate in monthly teleconferences to discuss the status of ongoing work. During the teleconference, the monthly reports shall also be discussed.
- Monthly Reports
  - o The contractor shall deliver monthly technical, financial, and schedule execution reports within 10 days following the first 30 days of the technical period of performance, and every 30 days thereafter through the technical period of performance. **(Deliverable Item 5.1)**
  - o Format: Contractor format is acceptable. MS Word shall be used for text documents, MS Excel shall be used for spreadsheet and graphic data, and MS PowerPoint shall be used for presentation material.

#### **4.2 Quarterly Status Reviews**

- The Contractor shall participate in Quarterly Status Reviews every 3 months to discuss the status of ongoing work. During the review, the quarterly reports shall also be discussed.
- Quarterly Reports
  - o The Contractor shall prepare a presentation that summarizes all of the project data and methods, and describes results and lessons learned in the previous quarter as well as the project objectives, approach and the desired outcomes for the following quarter. The Contractor shall deliver the presentation package in an appropriate electronic format seven (7) calendar days prior to the scheduled review. **(Deliverable Item 5.3)**
  - o Format: Contractor format is acceptable. MS Word shall be used for text documents, MS Excel shall be used for spreadsheet and graphic data, and MS PowerPoint shall be used for presentation material.

#### **4.3 Kick Off**

##### **4.3.1 Program Management Plan**

- The contractor shall deliver a Program Management Plan 5 days prior to the project Kick-Off meeting, review meetings, technical interchange meetings as designated by the government. **(Deliverable Item 5.6)**
- Format: Contractor format is acceptable. MS Word shall be used for text documents, MS Excel shall be used for spreadsheet and graphic data, and MS PowerPoint shall be used for presentation material.

#### **4.3.2 Kick Off Presentation**

- The Contractor shall prepare a PowerPoint presentation that facilitates review and discussion of the project objectives, approach (i.e., project schedule, milestones, deliverables), and the desired outcomes and tangible products. An electronic version of the Presentation shall be delivered to the COR at the time of the briefing. A copy shall also be delivered to the CO (preferably via email) not later than a week after the presentation. **(Deliverable Item 5.7)**
- Format: Contractor format is acceptable. MS Word shall be used for text documents, MS Excel shall be used for spreadsheet and graphic data, and MS PowerPoint shall be used for presentation material.

#### **4.4 Preliminary Design Phase**

This phase is used for the implementation of the design as described in the Kick-Off Meeting. Deliverables during this phase are listed in Table 5.3. This phase culminates with the Preliminary Design Review (PDR)

##### **4.4.1 Preliminary Design Review**

- The Contractor shall prepare a PowerPoint presentation that facilitates a preliminary design review and discussion for the test article conceptual design. Contractor shall deliver the presentation package in an appropriate electronic format seven (7) calendar days prior to the scheduled review. **(Deliverable Item 5.2)**
- Format: Contractor format is acceptable. MS Word shall be used for text documents, MS Excel shall be used for spreadsheet and graphic data, and MS PowerPoint shall be used for presentation material.

#### **4.5 Detailed Design Phase**

This phase is used for finalizing the chiplet design and the associated system software. Deliverables during this phase are listed in Table 5.4. This phase culminates with the Critical Design Review (CDR)

- Finalizing chiplet design and system software
- Critical Design Review (CDR)
  - o Present final chiplet design using RHBD libraries
  - o Present software designs
  - o Present packaging designs
  - o Present chiplet evaluation board design
  - o Present assured integrity strategy

##### **4.5.1 Critical Design Review**

- The CDR is used to present the final chiplet design using RHBD libraries, software designs, packaging designs, as well as the evaluation board design.
- The Contractor shall prepare a presentation in PowerPoint that facilitates a detailed design review and discussion for the test article. Contractor shall deliver the presentation package in an appropriate electronic format seven (7) calendar days prior to the scheduled review. **(Deliverable Reference 5.4)**
- Format: Contractor format is acceptable. MS Word shall be used for text documents, MS Excel shall be used for spreadsheet and graphic data, and MS PowerPoint shall be used for presentation material.

#### **4.6 Fabrication Phase**

- Chiplet fabrication using rad hard design specs
- Chiplet evaluation board fabrication and assembly

#### **4.7 Test and Characterization Phase**



- Test and characterize chiplet design in ambient conditions
- Final deliverables are listed in Table 5.5, including chiplet devices and populated evaluation boards
- The Final Review is used to review the final chiplet design and delivery, including all results and analysis during the design phases. This review is also used to review the evaluation board, as well as the test setup and configuration.
  - o The Contractor shall prepare a presentation in PowerPoint that facilitates a detailed design review and discussion for the test article. Contractor shall deliver the presentation package in an appropriate electronic format seven (7) calendar days prior to the scheduled review. **(Deliverable Reference 5.5)**
  - o Format: Contractor format is acceptable. MS Word shall be used for text documents, MS Excel shall be used for spreadsheet and graphic data, and MS PowerPoint shall be used for presentation material.

**Table 4.1**

The following shows the planned meetings, and its frequency/timeframe, duration, and location for this project:

Meeting	Frequency / Date	Duration	Location
Project Status Meetings	Monthly	4 Hrs	Via Telecon or Visit to Contractor Site
Preliminary Design Review	6 months after award	2 Days	Contractor
Quarterly Status Review	Quarterly every 3 months.	1 Day	Contractor
Critical Design Review	27 months after award	2 Days	Contractor
Final Review	45 months after award	2 Days	Contractor

## 5.0 Deliverables:

**Table 5.1**

The Contractor shall provide NASA with the following report/review deliverables:

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
5.1	4.3	Monthly Status Report	1	Monthly	TBD
5.2	4.4.1	Preliminary Design Review Presentation	1	1 Week prior to PDR	TBD
5.3	4.5	Quarterly Status Report	1	Quarterly every 3 months	TBD
5.4	4.6.1	Critical Design Review Presentation	1	1 Week prior to CDR	TBD
5.5	4.8	Final Presentation	1	1 Week prior to final deliveries	TBD

**Table 5.2**

The Contractor shall provide NASA with the following deliverables during the project Kick-off, prior to the start of the Preliminary Design Phase:

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
5.6	4.1	Program Management Plan	1	5 days prior to Kick-Off Meeting	Delivered to COR and CO electronically (preferably via email).
5.7	4.2	Kick-Off Presentation	1	Within 1 month after contract award  Date and time to be mutually agreed upon by the Contractor and COR.	See Task.

**Table 5.3**

The Contractor shall provide NASA with the following deliverables during the Preliminary Design Phase, culminating in the Preliminary Design Review:

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
5.8	4.4	High Level Conceptual Design of the Chiplet	1	PDR	TBD
5.9	4.4	Detailed Implementation Plan	1	PDR	See Task.
5.10	4.4	Detailed Schedule	1	PDR	See Task.
5.11	4.4	Theory of Operations Document	1	PDR	See Task.
5.12	4.4	Complete Listing of RHBD modules/cores that are planned for the chiplet design	1	PDR	See Task.
5.13	4.4	Analysis of Expected Upset Rate – For each functional block within the chiplet	1	PDR	See Task.
5.14	4.4	Analysis of Expected Failure Rate	1	PDR	Delivered to COR and CO electronically (preferably via email or DVD), and in accordance with NFS 1852.235-73 and contract.
5.15	4.4	Preliminary Timing Analysis	1	PDR	TBD
5.16	4.4	Preliminary Power Analysis	1	PDR	See Associated Tasks.
5.17	4.4	Preliminary Device Floor Plan	1	PDR	TBD

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
5.18	4.4	Package Concepts, with consideration to the high speed interfaces - Bare die - Packaged parts (i.e. CBGA, CCGA, etc)	1	PDR	TBD
5.19	4.4	Block Diagram of the FPGA-based design	1	PDR	TBD
5.20	4.4	Complete list of IP cores used for the FPGA-based design	1	PDR	TBD
5.21	4.4	Specifications and/or Conceptual Design for System Software	1	PDR	TBD
5.22	4.4	Detailed Block Diagrams of the Chiplet Evaluation Board Design	1	PDR	TBD
5.23	4.4	Assured Integrity Strategy	1	PDR	TBD

**Table 5.4**

The Contractor shall provide NASA with the following deliverables during the Detailed Design Phase, culminating in the Critical Design Review:

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
5.24	4.6	Software simulation and behavior models for the chiplet	2	9 months after the start of the Detailed Design Phase	TBD
5.25	4.6	FPGA-based Evaluation Boards	6	9 months after the start	TBD

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
		with a compiled chiplet design implemented and running		of the Detailed Design Phase	
5.26	4.6	All source code and results for the FPGA-based design	1	9 months after the start of the Detailed Design Phase	TBD
5.27	4.6	All source code and results of the software running on the FPGA-based evaluation board	1	9 months after the start of the Detailed Design Phase	TBD
5.28	4.6	Operating system, compiler, debugger used with the FPGA-based evaluation board	6	9 months after the start of the Detailed Design Phase	TBD
5.29	4.6	Updated High Level Conceptual Design of the Chiplet	1	CDR	TBD
5.30	4.6	Updated Implementation Plan	1	CDR	TBD
5.31	4.6	Updated Schedule	1	CDR	TBD
5.32	4.6	Updated Theory of Operations Document	1	CDR	TBD
5.33	4.6	Complete Listing of RHBD modules/cores that are planned for the chiplet design	1	CDR	TBD
5.34	4.6	Updated Analysis of Expected Upset Rate – For each functional block within the	1	CDR	TBD

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
		chiplet			
5.35	4.6	Updated Analysis of Expected Failure Rate	1	CDR	TBD
5.36	4.6	Updated Timing Analysis, showing sufficient margin at process/temperature corners	1	CDR	TBD
5.37	4.6	Updated Power Analysis	1	CDR	TBD
5.38	4.6	Detailed Package Drawings	1	CDR	TBD
5.39	4.6	Successfully synthesized full-up design of the chiplet using RHBD modules/cores	1	CDR	TBD
5.40	4.6	Chiplet Evaluation Board Schematics	1	CDR	TBD
5.41	4.6	Updated specifications and/or conceptual design for system software	1	CDR	TBD
5.42	4.6	Updated source code and results for the fully compiled chiplet design implemented on the FPGA within the FPGA-based evaluation board	1	CDR	TBD
5.43	4.6	Updated source code and results for the software running on	1	CDR	TBD

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
		the FPGA-based evaluation board			
5.44	4.6	Updated Operating System, compiler, debugger used to exercise the FPGA-based evaluation board	6	CDR	TBD
5.45	4.6	Assured Integrity Strategy	1	CDR	TBD

**Table 5.5**  
Final Deliverables:

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
5.46	4.8	Bare die	20	Final Delivery	TBD
5.47	4.8	Packaged chiplets	10	Final Delivery	TBD
5.48	4.8	Populated and tested evaluation boards, including any required test fixtures and specialty interface adapters	6	Final Delivery	TBD
5.49	4.8	All System Software, including: <ul style="list-style-type: none"> <li>- Boot software</li> <li>- Board Support Packages</li> <li>- Operating System</li> <li>- Self-test software</li> </ul>	6	Final Delivery	TBD

Item No.	Task Ref.	Deliverable Description	Qty.	Due Date	Delivery Instructions
5.50	4.8	All Development Software, including: - Compiler - Debugger	6	Final Delivery	TBD
5.51	4.8	Chiplet Datasheet, Specification, and User's Guide	1	Final Delivery	TBD
5.52	4.8	Evaluation Board User's Guide	1	Final Delivery	TBD
5.53	4.8	Final Analysis of Expected Upset Rate	1	Final Delivery	TBD
5.54	4.8	Final Analysis of Expected Failure Rate	1	Final Delivery	TBD
5.55	4.8	Final Power Analysis	1	Final Delivery	TBD
5.56	4.8	Final Timing Analysis	1	Final Delivery	TBD

## 6.0 HPSC Costed Options

The government team has defined the following options for which funding has not yet been secured, but which are highly desirable. Offerors will be encouraged to provide these costed options in their future proposal and to offer additional options that they feel would be advantageous to meet future govt. needs.

1. The addition of a third A53 processor cluster in the chiplet.
2. The inclusion of level 3 cache.
3. The addition of dual R5 processors for system management and real time critical computation.
4. The enhancement of the chiplet architecture to have two fault containment regions that are independently powered.
5. The provision of dual-port Time-Triggered Ethernet (TTE) and dual-port Spacewire interfaces.
6. The provision of a hermetically sealed package that is amenable to space qualification.



## Acronym List

[illegible]