Statement of Work Title:
A Multi-Pixel Delta-Sigma Modulated Laser Detection Circuit Realized in Standard CMOS

Primary Task
The contractor shall design and manufacture a delta-sigma modulation (DSM) based laser detection circuit based on government-furnished documentation. This is a mid-stage development effort. The contractor shall finalize the multi-channel manufacturing design based on the results of previous efforts. The award is fixed-price.

Long-Term Goal:
To develop a multi-channel laser detection circuit suitable for low-intensity optical sources operating in extreme temperature and radiation environments. In the long-term, this design will be ported to a more sophisticated process. To meet long-term project goals, the preferred partner will have demonstrable experience in both the present design process (ON Semiconductor C5 CMOS with hi-poly resistors and dual-poly capacitors) and the projected future process (Jazz Semiconductor SBC18 or SBC35 SiGe CMOS)

Statement of Work:
The effort involves the development of a CMOS integrated circuit containing multiple copies of the primary network of a single-pixel delta-sigma modulated laser detection circuit. The goal of this effort is to demonstrate the capability of multiple channels to measure independent signals while sharing common aspects of the network such as biasing. The design will be based upon government-provided information with modifications as mutually agreed upon during the course of development.

The project involves the design, analysis, and layout of an integrated circuit (IC) using standard CMOS process technology. The vendor shall perform design, layout, simulation, and post-manufacturing testing of performance measures of the networks on the IC using design tools suitable for integrated circuit design and development. Such tools at a minimum shall include circuit simulation at the device level, Design-Rule-Check (DRC), Layout-vs-Schematic (LVS), and parasitic extraction from layout. These are basic and necessary capabilities.

Additional sub-networks may be required as individual test platforms; type and number to be determined and defined during detailed analysis performed by the contractor. Proposals for the potential sub-networks are to be reviewed and approved by the government.

Additional testing will be performed at NASA Langley Research Center.

The contractor shall package the test die in standard plastic or ceramic packages of a size to be determined at the mid-design review. The contractor shall perform primary functional testing of die. Among the basic tests will be operation at nominal supply voltage, nominal supply current at nominal voltage, test-to-destruction of supply voltage range, operation under nominal supply voltage range, nominal output response vs. input stimulus, and channel-to-channel interaction. Other tests may be suggested during the development process.

The contractor shall design and fabricate the IC using the ON Semiconductor C5 manufacturing process. It is suggested but not required that such processing be organized through MOSIS to maintain compatibility with the government's efforts on this project.

Milestones:

1. Design, fabricate, and test the prototype ICs built upon the ON Semiconductor C5 0.5 μm process. Design will be ready for submission to foundry on or before the dates required by the foundry but no later than Dec 31, 2015[1].

2. Compilation of test results shall include critique of as-tested design and suggestions for future design improvements.

Deliverables:

1. Projected contractor schedule of events and development activities

2. Progress reports preliminary to each NASA site participation. Anticipated time frames include TBD (kickoff), TBD (mid-term design review), TBD (final design review), TBD (test review meeting)

3. Design files for all network designs including but not limited to:
   a. design analyses,
   b. simulation circuits and model listings,
   c. layout design files in GDSII format
   d. extracted simulation netlists in text file,
   e. design rule check files and results,
   f. layout vs. schematic check files and results[2]

4. Physical die as delivered from manufacturer. The set of die should be split approximately in half between unpackaged and packaged parts. It is expected that several die will be lost to test-to-destruction procedures; the quantity of delivered product should be evenly divided with one half being delivered to NASA

5. Description of test goals, system configuration, test simulation/operation files, and test results, including raw data in a platform-independent format.

6. Detailed engineering report to address:

   a. Highlights of design and development in summary form;
   b. Test reports describing methodologies, tools, and results of test data reduction in form of tables or charts as appropriate.

[1] Fabrication schedules are set far in advance. Selecting a specific target date will need to be deferred until initial discussions with lead investigator

[2] Schematic files should be in platform-independent text format. Layout files should be presented in an appropriate platform-independent format including but not limited to the GDSII format.

c. Conclusions and critiques of final manufactured design, suggestions for future improvement, and
d. Considerations related to conversion of project to more advanced process such as Jazz Semiconductor SBC18/35.

It is anticipated that NASA personnel will attend critical design reviews at contractor's facilities on dates suggested by Deliverables(1). Specific dates shall be determined as necessary during the development of this project.

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Government Furnished Information

NASA will provide current-status schematics, models, and preliminary layout diagrams with the understanding that this information is provided as a preliminary guideline. The vendor will have access to more detailed foundry information with which to refine the design for manufacturing