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ICE, CLOUD, and Land Elevation Satellite (ICESat-2) Project

Radiation Requirements Document (RRD) ICESat-2-SMA-REQ-0037

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Goddard Space Flight Center
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CHANGE RECORD PAGE

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1.0 Introduction

This document provides the ICESat-2 project with requirements for Total Ionizing Dose (TID), non-ionizing Displacement Damage Dose (DDD), and Single-event Effects (SEE). These requirements are derived from analysis information contained in the Radiation Environment Description Document (ICESat-2-SMA-ANYS-0125). ICESat-2-SMA-ANYS-0125 covers the original launch date of November 2014 in detail and the update launch date of February 2016 briefly. After further analysis, it was decided that the change in launch date did not alter the external spacecraft radiation environment enough to warrant a complete revision to the original radiation environment description document since the mission total ionizing dose increased by less than 2 krad(Si). This increase has been added to the top-level total ionizing dose requirement.

This document also defines the waiver process to be followed if the radiation requirements in this document (ICESat-2-SMA-REQ-0037) are not satisfied.

1.1 Definitions

Single-Event Effect (SEE) - any measurable effect to a circuit due to an ion strike. This includes, but is not limited to single-event upsets (SEUs), single-event transients (SETs), single-hard errors (SHEs), single-event latchups (SELs), single-event functional interrupts (SEFIs), single-event burnouts (SEBs), single-event gate ruptures (SEGRs), and single-event dielectric ruptures (SEDRs).

Single-Event Upset (SEU) - a change of state or transient induced by an energetic particle such as a cosmic ray or proton in a device. This may occur in digital or analog circuits and may have effects in surrounding interface circuitry (a subset known as SETs). These are “soft” errors in that a reset or rewriting of the device will usually return the device to normal behavior thereafter. The general goal for non-destructive events such as SEUs or SETs is not to avoid them completely, but to manage their impact through robust circuit design, automatic correction, and/or operational activities based on knowledge from ground radiation tests and circuit/system analysis.

Single Hard Error (SHE) - a SEU that causes a permanent change to the operation of a device. An example is a stuck bit in a memory device.

Multiple Bit Upset (MBU) - an event induced by a single energetic particle such as a cosmic ray or proton that causes multiple upsets or transients during its path through a device or system in a single logical structure (ex., 2 bits affected in a single 16-bit word).

Single-Event Functional Interrupt (SEFI) - a condition that causes loss of device functionality due to a single event in a control portion of a device. It generally requires a device reset or a re-initialization to resume normal device operations, but for some devices, a power cycle is necessary to resume normal device operations. The general goal

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for non-destructive events such as SEFI is to avoid them, however, managing their impact through robust circuit design, automatic correction, and/or operational activities may be considered.

Single-Event Latchup (SEL) - a condition that may cause device failure due to a single-event induced high-current state. A SEL may or may not cause permanent device damage, but requires power cycling of the device to resume normal device operations. In addition, susceptible devices have the concern for latent damage, where the device does not fail from the immediate single particle event, but reliability is degraded and premature failure may occur.

Single-Event Burnout (SEB) - a condition that can cause device destruction due to a high-current state in a power transistor.

Single-Event Gate Rupture (SEGR) - a destructive single ion induced condition in power MOSFETs that may result in the formation of a conducting path in the gate oxide.

Linear Energy Transfer (LET) - a measure of the energy deposited per unit length as an energetic particle travels through a material. The common LET unit is $(\mathrm{MeV \cdot cm^2})/\mathrm{mg}$, which is the energy loss per unit path length divided by the material density, usually given as $\mathrm{mg/cm^3}$.

Threshold LET (LET_{th}) - the maximum LET at which no SEE is observed at a particle fluence of 10^7 ions/cm^2.

Non-Ionizing Energy Loss (NIEL) - a measure of the rate of energy loss due to atomic displacements as a particle traverses a material.

Total Ionizing Dose (TID) – the mean energy deposited by ionizing radiation in a device region divided by the mass of the region. This is often given in units of rad(Si), where 1 rad(Si) = 100 erg deposited per gram of silicon.

Enhanced Low Dose Rate Sensitivity (ELDRS) – used to refer to a bipolar or BiCMOS part that shows enhanced (greater) radiation induced damage for a fixed dose at dose rates below about 50 rad(Si)/s compared to damage at the same dose for dose rates of > 50 rad(Si)/s. The enhancement may be a result of true dose rate effects or time dependent effects, or both.

Displacement Damage Dose (DDD) – the mean energy deposited by ionizing radiation in a device region that goes into atomic displacements divided by the mass of the region. There is no official unit for DDD. One such unit is MeV/g.

Radiation Design Margin (RDM) – the mean (often geometric mean) of the radiation failure level of the part, R_{mf}, divided by the radiation specification level, R_{spec}.

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2.0 Total Ionizing Dose

No effect due to TID shall cause permanent damage to, or performance degradation of the flight system. Degradation of individual components shall be included in appropriate worst case analyses.

2.1 TID Level Requirements

All EEE parts shall be able to tolerate a minimum TID of 15 krad(Si). This is a RDM of 2 based on the top-level mission TID for a 5-year mission with a 600 km circular orbit at a 94° inclination as described in the Radiation Environment Description Document mentioned in Section 1.0. The assumed launch date is in February 2016. Note that this TID requirement was computed based on 2.54 mm (100 mil) of solid spherical (4π sr) aluminum shielding and a dose-depth curve. As described below, different shielding environments, and available test data may change this requirement.

Lower dose levels may be used when approved by the Parts Control Board (PCB). Justification for using lower doses shall identify the physical location of the part being submitted for approval and a dimensioned drawing to provide context and a clear description of the justification logic. This information shall be provided as a part of the radiation report. If the waiver is obtained, subsequent design adjustments that significantly increase the dose inside the box shall invalidate the waiver. Such design adjustments may include, but are not limited to, repositioning the box or thinning the box wall(s).

Parts with a die-level TID tolerance less than 1.2 krad(Si) for lot specific data, and 2.4 krad(Si) for generic data, shall be prohibited in all circumstances.

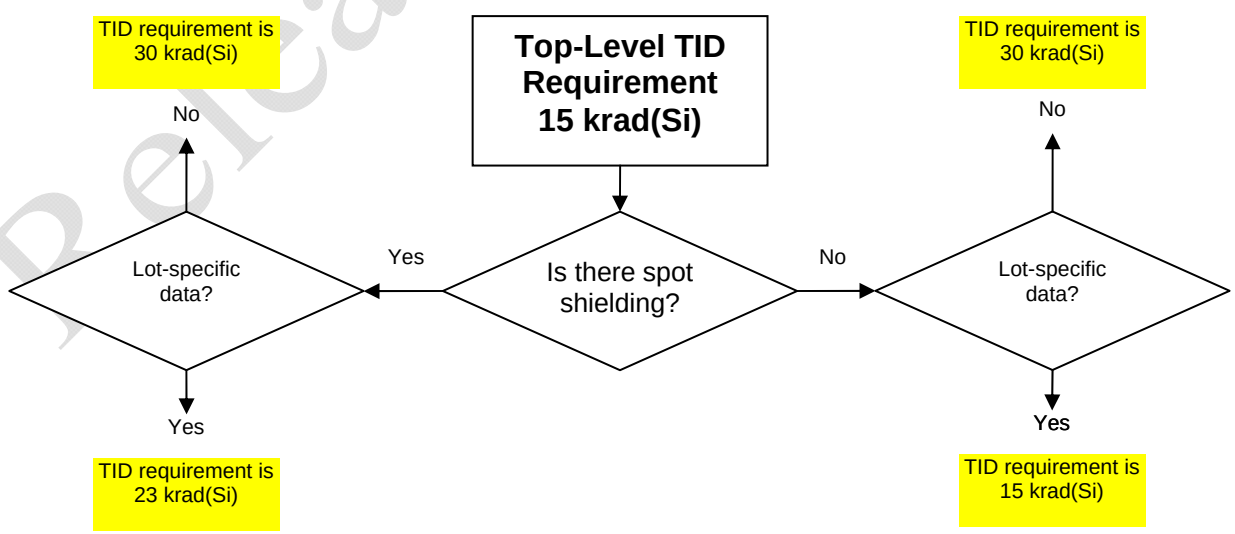

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Figure 1: Component TID decision chart including considerations for spot shielding and the availability of lot-specific radiation data. Note that levels are computed based on base level TID of 7.5 krad(Si). The top-level requirement includes the mandatory 2x RDM.

2.2 Spot Shielding Margin Requirements (including Rad-PAK)

The use of spot shielding shall be approved by the PCB. If necessary and approved, appropriate spot shielding may be added around a component so that the part can meet the shielded dose. When spot shielding is used, a minimum RDM of 3*x* shall be imposed.

Due to the nature of the radiation environment, the use of spot shielding on parts is discouraged. Requests to use spot shielding shall require additional evaluation (to include application) by the PCB. Parts with a die level TID tolerance less than 23 krad(Si), an RDM of 3, shall be prohibited in the presence of spot shielding.

See Figure 1 for TID requirement decision chart.

2.3 TID Test Data Requirements

Flight lot testing shall be mandatory if part test data (same part number, same manufacturer, and same process) do not exist.

Flight lot testing shall be mandatory for commercial (non-Defense Supply Center Columbus (DSCC) audited) parts, even if generic data exist.

Generic radiation data for a part with the same part number, manufacturer and process shall be submitted to the PCB for evaluation. Acceptable data from 3 or more lots shall have a RDM of 4*x* (30 krad(Si)) assigned to the application. Use of data from less than 3 lots is discouraged but will be considered on a case by case basis. See Figure 1 for TID requirement decision chart.

Testing shall be required on the flight procurement lot in order to use the 2*x* design margin based in section 2.1 on page 8 of this document. Flight lot testing is always preferred.

All TID testing shall be ^{60}Co testing as per Test Method Standard, Microcircuits (MIL-STD-883, Method 1019.7). Guaranteed devices from the vendor may use an x-ray source for lot qualification.

2.4 Requirements for Parts with Enhanced Low Dose Rate Effects

Parts based on bipolar or BiCMOS technology shall be evaluated for Enhanced Low Dose Rate Sensitivity (ELDRS) effects. Test data used to justify use of bipolar or BiCMOS components shall have been collected from tests conducted at dose rates ≤ 0.01 rad(Si)/s, based on MIL-STD-883 Method 1019, unless it can be demonstrated by

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process information or comparative test data that no dose rate enhancement effect exists for the parameters of interest.

If data are taken on flight lot parts that exhibit ELDRS effects at dose rates > 0.01 rad(Si)/s, the PCB shall evaluate the data to determine acceptability for flight. A minimum test data requirement in this case is to obtain data to a total dose of at least 53 krad(Si) or to a RDM of at least 7*x*.

3.0 Displacement Damage Dose

No effect due to Displacement Damage Dose (DDD) shall cause permanent damage to, or performance degradation of the flight system. Degradation of individual components shall be included in appropriate worst case analyses.

3.1 DDD Level Requirements

DDD requirements for parts are material dependent and shall be for an equivalent 10 MeV proton fluence.

All silicon EEE parts shall be able to tolerate either a minimum 10 MeV equivalent proton fluence of 1.2×10^{10} cm^{-2}, an RDM of 2, or the equivalent fluence obtained from the table of silicon values in section 3.3.1, whichever fluence is greater. A RDM of 2*x* must be applied to the fluences provided in the table.

All gallium arsenide EEE parts shall be able to tolerate either a minimum 10 MeV equivalent proton fluence of 1.4×10^{10} cm^{-2} or the equivalent fluence obtained from the table of gallium arsenide values in section 3.3.1, whichever fluence is greater. A RDM of 2*x* must be applied to the fluences provided in the table.

Alternative proton energies can be used for test and analysis by scaling according to the Non Ionizing Energy Loss (NIEL) as in Summers, G.P., et. al., *IEEE Trans. Nuc. Sci.*, vol. 40, no. 6, pp. 1372-1379, 1993. See section 3.3.1.

Use of equivalent fluences below the maximum equivalent fluence in the box shall require approval by the PCB. Justification methodology is described in the last paragraph in section 2.1.

3.2 Spot Shielding Margin Requirements

The use of spot shielding shall be approved by the PCB. If necessary and approved, appropriate spot shielding may be added around a component so that the part can meet the shielded equivalent fluence. When spot shielding is used, a minimum RDM of 3*x*, or 19.5 krad(Si), shall be imposed.

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Due to the nature of the radiation environment, the use of spot shielding on parts is discouraged. Requests to use spot shielding shall require additional evaluation (to include application) by the PCB.

3.3 DDD Test Data Requirements

Flight lot testing shall be mandatory if test data (same part number, same manufacturer, and same process) do not exist for parts susceptible to displacement damage.

Flight lot testing shall be mandatory for commercial (non-DSCC audited) parts, even if generic data exist.

Generic radiation data for a part with the same part number, manufacturer and process shall be submitted to the PCB for evaluation. Acceptable data from 3 or more lots shall have a RDM of 4*x* assigned to the application. Use of data from less than 3 lots is discouraged but will be considered on a case by case basis.

Testing shall be required on the flight procurement lot in order to use the 2*x* margin provided in the ray trace analysis. Flight lot testing is always preferred.

Note that makers of flight optocoupler devices frequently procure their optocouplers from commercial sources with poor process control. As such, use of generic data to justify the use of optocouplers is strongly discouraged. If generic data are proposed for use, a waiver must be filed with adequate technical justification. Such justification shall at least include evidence that the LED fabrication process has not been changed since the existing data were taken. Additional margin beyond RDM of 2*x* shall be imposed by the PCB.

3.3.1 Use of Equivalent Proton Fluences for DDD Testing

Use the shielding thickness in the following tables to obtain a proton fluence that produces displacement damage equivalent to that seen in that location during the ICESat-2 mission. It is acceptable to test to that equivalent fluence with the appropriate margin applied. The equivalent fluences in the following two tables do not include design margins. The first table gives results for silicon devices and the second table for gallium arsenide devices. Devices composed of other materials will be considered on a case by case basis.

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Table1: Equivalent Fluences In Silicon For ICESat-2 (No Margin)

Aluminum Solid-Sphere Shield Thickness			1 MeV Equivalent Proton Fluence #/cm^2	10 MeV Equivalent Proton Fluence #/cm^2	50 MeV Equivalent Proton Fluence #/cm^2	63 MeV Equivalent Proton Fluence #/cm^2
mm	g/cm^2	mils				
0.037	0.01	1.46	3.18E+10	2.71E+11	5.52E+11	6.35E+11
0.047	0.013	1.85	2.75E+10	2.35E+11	4.77E+11	5.49E+11
0.059	0.016	2.32	2.18E+10	1.86E+11	3.79E+11	4.36E+11
0.074	0.02	2.91	1.74E+10	1.48E+11	3.01E+11	3.47E+11
0.093	0.025	3.66	1.39E+10	1.18E+11	2.41E+11	2.77E+11
0.117	0.032	4.61	1.08E+10	9.24E+10	1.88E+11	2.16E+11
0.148	0.04	5.83	8.38E+09	7.15E+10	1.45E+11	1.67E+11
0.186	0.05	7.32	7.31E+09	6.23E+10	1.27E+11	1.46E+11
0.234	0.063	9.21	5.95E+09	5.08E+10	1.03E+11	1.19E+11
0.294	0.079	11.57	4.66E+09	3.98E+10	8.09E+10	9.31E+10
0.371	0.1	14.61	3.75E+09	3.20E+10	6.50E+10	7.49E+10
0.466	0.126	18.35	3.12E+09	2.67E+10	5.42E+10	6.24E+10
0.587	0.158	23.11	2.50E+09	2.13E+10	4.34E+10	4.99E+10
0.739	0.2	29.09	2.03E+09	1.73E+10	3.51E+10	4.04E+10
0.931	0.251	36.65	1.64E+09	1.40E+10	2.84E+10	3.27E+10
1.172	0.316	46.14	1.35E+09	1.15E+10	2.34E+10	2.69E+10
1.475	0.398	58.07	1.12E+09	9.59E+09	1.95E+10	2.25E+10
1.857	0.501	73.11	9.17E+08	7.82E+09	1.59E+10	1.83E+10
2.338	0.631	92.05	7.53E+08	6.42E+09	1.31E+10	1.50E+10
2.943	0.794	115.87	6.17E+08	5.27E+09	1.07E+10	1.23E+10
3.705	1	145.87	5.13E+08	4.38E+09	8.91E+09	1.03E+10
4.665	1.259	183.66	4.35E+08	3.71E+09	7.54E+09	8.68E+09
5.872	1.585	231.18	3.84E+08	3.28E+09	6.67E+09	7.67E+09
7.393	1.995	291.06	3.34E+08	2.85E+09	5.79E+09	6.67E+09
9.307	2.512	366.42	2.94E+08	2.51E+09	5.10E+09	5.88E+09
11.717	3.162	461.30	2.62E+08	2.24E+09	4.55E+09	5.23E+09
14.751	3.981	580.75	2.32E+08	1.98E+09	4.03E+09	4.64E+09
18.57	5.012	731.10	2.04E+08	1.74E+09	3.55E+09	4.08E+09
23.378	6.31	920.39	1.76E+08	1.50E+09	3.05E+09	3.51E+09
29.432	7.943	1158.74	1.49E+08	1.27E+09	2.58E+09	2.98E+09
37.052	10	1458.74	1.31E+08	1.12E+09	2.28E+09	2.62E+09

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Table2: Equivalent Fluences In Gallium Arsenide For ICESat-2 (No Margin)

Aluminum Solid-Sphere Shield Thickness			1 MeV Equivalent Proton Fluence #/cm^2	10 MeV Equivalent Proton Fluence #/cm^2	50 MeV Equivalent Proton Fluence #/cm^2	63 MeV Equivalent Proton Fluence #/cm^2
mm	g/cm^2	mils				
0.037	0.01	1.46	3.11E+10	2.55E+11	4.48E+11	4.58E+11
0.047	0.013	1.85	2.68E+10	2.19E+11	3.86E+11	3.94E+11
0.059	0.016	2.32	2.12E+10	1.74E+11	3.05E+11	3.12E+11
0.074	0.02	2.91	1.68E+10	1.38E+11	2.42E+11	2.47E+11
0.093	0.025	3.66	1.34E+10	1.10E+11	1.93E+11	1.98E+11
0.117	0.032	4.61	1.04E+10	8.56E+10	1.50E+11	1.54E+11
0.148	0.04	5.83	8.09E+09	6.63E+10	1.16E+11	1.19E+11
0.186	0.05	7.32	7.07E+09	5.79E+10	1.02E+11	1.04E+11
0.234	0.063	9.21	5.77E+09	4.73E+10	8.31E+10	8.49E+10
0.294	0.079	11.57	4.55E+09	3.73E+10	6.56E+10	6.70E+10
0.371	0.1	14.61	3.71E+09	3.04E+10	5.35E+10	5.46E+10
0.466	0.126	18.35	3.13E+09	2.56E+10	4.50E+10	4.60E+10
0.587	0.158	23.11	2.54E+09	2.08E+10	3.66E+10	3.74E+10
0.739	0.2	29.09	2.10E+09	1.72E+10	3.02E+10	3.09E+10
0.931	0.251	36.65	1.74E+09	1.43E+10	2.50E+10	2.56E+10
1.172	0.316	46.14	1.47E+09	1.20E+10	2.11E+10	2.16E+10
1.475	0.398	58.07	1.26E+09	1.03E+10	1.81E+10	1.85E+10
1.857	0.501	73.11	1.06E+09	8.72E+09	1.53E+10	1.57E+10
2.338	0.631	92.05	9.07E+08	7.43E+09	1.31E+10	1.33E+10
2.943	0.794	115.87	7.77E+08	6.37E+09	1.12E+10	1.14E+10
3.705	1	145.87	6.75E+08	5.53E+09	9.72E+09	9.94E+09
4.665	1.259	183.66	5.93E+08	4.86E+09	8.54E+09	8.72E+09
5.872	1.585	231.18	5.38E+08	4.41E+09	7.75E+09	7.91E+09
7.393	1.995	291.06	4.83E+08	3.96E+09	6.95E+09	7.11E+09
9.307	2.512	366.42	4.36E+08	3.57E+09	6.28E+09	6.41E+09
11.717	3.162	461.30	3.97E+08	3.25E+09	5.71E+09	5.83E+09
14.751	3.981	580.75	3.57E+08	2.93E+09	5.14E+09	5.26E+09
18.57	5.012	731.10	3.20E+08	2.62E+09	4.61E+09	4.71E+09
23.378	6.31	920.39	2.81E+08	2.31E+09	4.05E+09	4.14E+09
29.432	7.943	1158.74	2.44E+08	2.00E+09	3.52E+09	3.59E+09
37.052	10	1458.74	2.15E+08	1.76E+09	3.09E+09	3.16E+09

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4.0 Single-Event Effects

4.1 Non-Destructive Events: SEU, SET, SEFI, SHE, and MBU

All components shall be designed to avoid or tolerate errors due to non-destructive SEUs.

No permanent loss of function shall result due to non-destructive SEUs.

Flight lot testing shall be mandatory if part test data (same part number, same manufacturer, and same process) do not exist.

Flight lot testing shall be mandatory for commercial (non-DSCC audited) parts, even if generic data exist.

There is no minimum LET threshold (LET_{th}) imposed for devices that show non-destructive single-event effects (SEE). However, devices with $LET_{th} > 20$ (MeV·cm^2)/mg are recommended to reduce system risks.

Components with a SEE $LET_{th} < 20$ (MeV·cm^2)/mg shall be evaluated for both heavy ion and proton sensitivity. The evaluation shall include the criticality and the rate of the event. Further information on event criticality is found at http://radhome.gsfc.nasa.gov/radhome/papers/seecai.htm. Rate calculations shall use the fluence spectra described in Section 4.4. Rates shall be given for normal quiet times and during a worst case solar event.

Components with a SEE 20 (MeV·cm^2)/mg $\leq LET_{th} \leq$ 75 MeV-cm^2/mg shall be evaluated for heavy ion sensitivity. The evaluation shall include the criticality and the rate of the event. Rates shall be given for normal quiet times and during a worst case solar event.

Components with an SEE LET threshold > 75 (MeV·cm^2)/mg need no further evaluation.

Single-events that do not propagate to a detectable level (analog transients that are filtered by the downstream circuitry, momentary corruption of non-critical or over-sampled engineering telemetry or single word science loss, for example) shall not require rate calculation. Justification for not calculating rates shall be provided in the radiation analysis.

Propagating single-event effects may be defined as serious or critical. Serious single-event effects are those that are handled locally by mitigation approaches such as EDAC, programmed scrub, etc. Critical single-event effects are those that require ground intervention to correct.

The rate for propagating single-event effects shall be calculated. An evaluation shall be conducted to ensure that the mitigation techniques for serious single-event effects are

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sufficient to keep them from becoming critical. (*i.e.*, the rate of mitigation shall be sufficient to clear serious single-event effects before an additional error occurs that requires ground intervention). System radiation test validation is suggested, but analysis may be sufficient.

The rate of critical single-event effects shall be < 1 per 10 years.

Test Data Requirements:

Tests for SEU shall be done at a bias of $0.90 \cdot V_{dd}$ or $0.95 \cdot V_{dd}$. The bias should be chosen so the device remains within its specifications.

4.2 Destructive Events: SEL

All SEL events (including high current events where functionality can be restored by power cycling) shall be considered potentially destructive and treated in the same manner.

All devices shall have LET thresholds for SEL greater than 37 $(MeV \cdot cm^2)/mg$.

For devices with SEL thresholds between 37 $(MeV \cdot cm^2)/mg$ and 75 $(MeV \cdot cm^2)/mg$:

- An evaluation of the probability and impact of destructive events shall be conducted.
- When the rate of a destructive SEL at the part level is > 1 per 100 years, circumvention (the event still occurs, but the effect is minimized) shall be implemented such that said SEL will not adversely affect full mission success. Probability calculations shall use the fluence spectra described in Section 4.4.
- Circumvention techniques shall be evaluated to ensure that no latent damages are induced by an event in the devices prior to correction. This requires radiation test and failure analysis as per NASA Alert NA-GSFC-2005-05, included in this document as Appendix A. This requires current density analysis and testing to verify devices are latent damage free.

For devices with SEL thresholds > 75 $(MeV \cdot cm^2)/mg$, no additional analysis is necessary.

Test Data Requirements:

SEL testing shall be done under "worst case" conditions. This requires the device to be tested at a temperature of 80° C and a bias of $1.05 \cdot V_{dd}$ or $1.10 \cdot V_{dd}$. The bias should be chosen so the device remains within its specifications.

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4.3 Destructive Events: SEB and SEGR

All power transistors shall have a SEGR and SEB threshold LET > 37 (MeV·cm^2)/mg when biased at 133% of the application V_{ds} or V_{ce}. Note that if the application requires a large number of power transistors, it may still carry some risk for LETs > 37 (MeV·cm^2)/mg despite use of de-ratings.

Test data requirements:

Ground testing on the flight lot shall be required for any commercial device.

SEGR test data must be taken and/or interpreted with care: the safe-operating area (SOA) of a MOSFET must be determined by data taken at normal beam-incidence only; in addition, the SOA is sensitive to the energy of the ion, not just LET, due to the interplay of ion range and LET and resultant energy transfer to the sensitive region (see Titus, J.L., and Wheatley, C.F. *IEEE Trans. Nucl. Sci.*, vol. 50, no.6, pp. 2341-2351, 2003 and Liu, S., et al., *IEEE Trans. Nucl. Sci.*, vol. 55, no.6, pp. 3122-3129, 2008.)

For all SEE radiation hardened devices tested with appropriate ion energies and LETs, the test data shall be considered usable provided:

- The process and foundry are the same as the flight lot
- Tests were done on the flight lot or Military Specification parts will be flown
- LET > 37 (MeV·cm^2)/mg data are included

MOSFET and BJT de-rating:

MOSFETs and BJTs shall be de-rated to 75% of the highest passing V_{ds} or V_{ce} as determined by ground test data at LET > 37 (MeV·cm^2)/mg (see note on ion energy under test data requirements above).

Note: Typically, a particle fluence of 10^5 ions/cm^2 is used for SEB and SEGR testing.

4.4 Space Rate Calculations

The environment for SEE rate calculations is specified in document ICESat-2-SMA-ANYS-0125, Radiation Environment Description Document for the ICESat-2 Mission. The heavy ion environment for quiet conditions is given in Figure 6 and Table A6. Worst case conditions during a solar particle event are given in Figure 7 and Tables A7a and A7b. It is not acceptable to use the geosynchronous orbit obtained from CREME96 (https://creme96.nrl.navy.mil/) for these heavy ion calculations. The trapped proton

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environment for a worst case orbit average and the peak flux are given in Figure 8 and Table A8. Alternatively, the orbit-averaged and peak trapped proton spectra obtained from the AP8MIN model in CREME96 may be used. Orbit parameters to be used are perigee = 600 km, apogee = 600 km, angle of inclination = 94°, initial longitude of ascending node = 0 degrees, initial displacement from ascending node = 0 degrees, displacement of perigee from ascending node = 0 degrees, and number of orbits = 100. Worst case conditions for solar protons are given in Figure 9 and Table A9. It is not acceptable to use the geosynchronous orbit obtained from CREME96 for solar protons. In all rate calculations, it is acceptable to assume 2.54 mm (100 mil) of aluminum shielding in solid sphere geometry.

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APPENDIX A: NASA Advisory NA-GSFC-2005-05

Goddard Space Flight Center	GSFC NASA ADVISORY

1. NA-GSFC-	**2.** Latent Damage Reliability Issues Due to Single-Event Latchup and High-Current Error Modes.	
3. Manufacturer N/A	**4.** N/A	**5. Federal Stock Code** N/A
6. N/A	**7. Lot Date** N/A	**8. Controlling Spec/Document Number** N/A

9. References
Becker et al., "Latent Damage in CMOS Devices From Single-Event Latchup," IEEE Trans. Nucl. Sci., vol. 49, no. 6, p. 3009

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11. Problem Description and Details:
When parts experience an overcurrent due to Single-Event Latchup (SEL) or other single-event effects (SEE), they may fail outright, they may suffer no damage, or they may remain functional despite having sustained "latent damage" that compromises their future reliability. This last possibility is a concern not just because of the threat it poses to part reliability, but also because it blurs the line between destructive and nondestructive SEE and because it can be very difficult and costly to determine whether a part is vulnerable to latent damage. It is important to stress that parts may sustain latent damage even if SEL detection and recovery circuitry is used. Properly addressing this threat requires both proper test procedure and proper investigation of parts after they have been tested. Finally, the facts that the study of latent damage is in its infancy and that state-of-the-art microelectronics continues to introduce new materials and device structures ensures that best practice for handling this threat will evolve rapidly. Pages 2 and 3 give additional details on contemporary best

12. Actions Recommended:

(1) All spacecraft electronic system/subsystem designers should consult with the radiation effects engineers early in the design stage to ensure that parts potentially susceptible to SEL and latent damage are identified for testing and evaluation.

(2) Because latent damage is a relatively new threat, even "heritage" parts that exhibit "nondestructive" SEL should be evaluated for potential susceptibility.

(3) Even parts with external SEL circumvention circuitry should be evaluated for latent damage issues.

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1. Advisory Number	**2. Subject**

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NA-GSFC-2005-05	Latent Damage Reliability Issues Due to Single-Event Latchup and High-Current Error Modes.

11. Problem Description and Details: *(Continued from page 1)*

Latent Damage: Best Test and Analysis Practice for Managing Risks

Latent damage may occur any time parts experience an error mode with sufficiently high current that part reliability is compromised due to thermal stress, electromigration or other mechanisms. The most common triggering mechanism is Single-Event Latchup (SEL), although high current single-event functional interrupts (SEFIs) and other SEE modes may also give rise to currents sufficiently high to be of concern. Latent damage poses a concern not just because it may compromise device reliability, but also because it blurs the line between "destructive" and "nondestructive" SEL. The microscopic evidence of latent damage observed by Becker et al.[1] means that it is no longer sufficient that a SEL susceptible part remain functional after SEL. The prospect of latent damage also complicates other aspects of testing for potentially destructive SEE. For example, just as multiple SEL modes in a part may divide between destructive and nondestructive, some "nondestructive" modes may result in latent damage while others do not. Thus, a single dwell test, in which the part is left in a high-current SEL state for several minutes may not be sufficient to allay all latent damage concerns.
We stress that the study of latent damage is still nascent, so it is not possible to state with 100% certainty what threshold current or other characteristics an event must reach to be of concern. The study by Becker et al. found that in the parts that exhibited latent damage (Analog Devices AD9260 and National Semiconductor ADC10231 analog to digital converters and the Cardinal/Cypress CAR/CPPXIT-A7BR oscillator), the current density during SEL exceeded 1.0E7 A/cm^2. However, this study relied on visual evidence (optical microscopy or SEM) of damage (e.g. melted metallization, cracked dielectrics), and some damage may result in compromised reliability without a clear visual manifestation. Moreover, current density is not a direct observable, and must usually be calculated by dividing the peak power supply current by the minimum metallization cross section. Since test hardware may not always capture the peak current and accurate information on metal-trace cross-sectional areas may not be available, it is better to err on the side of caution. For these reasons, we place the threshold for concern at 1.0E6 A/cm^2, subject to revision as this threat is better understood.

Current Best Practice

Current best practice with regard to detection of latent damage susceptibility affects both testing and post-test procedure. With regard to testing, the main concern is that all SEL (or other SEE) modes that may be capable of causing latent damage be detected. This means that irradiating the part until one has observed SEL a few times may not be sufficient. Instead, one should irradiate parts to a predetermined fluence dictated by the acceptable failure rate and confidence level for the mission. In addition, however, one should at the very least seek to categorize the SEL modes of the part (in terms of maximum latchup current, current rise time, etc.) to determine whether different SEL modes are present and conduct a dwell test of several minutes for each SEL mode detected. Alternatively, it may be possible to detect the different SEL modes during heavy-ion testing and then conduct dwell tests using laser irradiation. In addition, several tools may be useful in characterizing various SEL modes—especially in conjunction with laser irradiation. Infrared microscopy can identify "hotspots" on the part that may indicate high thermal stress due to overcurrent conditions. In addition, Kuboyama et al.[2] have suggested use of photo-emission microscopy to detect optical photon emission that occurs due to recombination during an SEL—a means of distinguishing SEL from other high-current error modes. Such techniques may be useful not just for detecting high-current error modes but also for determining whether the high currents are carried over the entire part or are localized to a particular metal trace.
Following the above guidelines will ensure with high confidence that any vulnerability to either destructive SEL or to latent damage is realized during testing. However, one must still detect any latent damage that has occurred. The following is recommended for latent damage testing of samples after SEL testing:

1) Optical microscopy of the device (500x min, 1000x preferred)
2) Life tests with associated failure analyses
3) Thermal cycling (full-functional)
4) Maximum rating test and analysis (drive device to maximum rated limits to look for "hot spots"; use an un-irradiated device as a reference; techniques such as infrared camera or liquid crystal film might be used to detect such hot spots)
5) Repeat microscopic examination (500x min, 1000x preferred)
6) Full functionality test
7) Scanning electron microscopy (SEM)

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11. Problem Description and Details: *(Continued from page 2)*

These tests are intended to observe any latent damage that may have occurred and/or activate it so that it can be detected. Unfortunately, the process of SEE testing can itself be stressful for the parts, since even for hermetically sealed parts the package cover must be removed from the package, exposing the parts to the atmosphere and other stresses. For plastic encapsulated parts, flip-chips and other advanced packages, the stresses can be even more severe, since preparation may involve removal of the die from the package, thinning of the die and so on. In such cases, it may be difficult to determine whether the cause of any degraded performance in the life test is radiation induced or results from the pre-irradiation handling of the parts. Careful part handling, including provision of a dry nitrogen environment for parts may limit damage due to environmental factors, but this significantly increases test costs. However, to distinguish definitively between damage caused by radiation-induced overcurrent and that caused by pre-processing of the devices, it may be necessary to compare performance on the above tests for two groups of parts—the post SEL parts and a control group that has gone through the same pre-irradiation processing, but not been irradiated. Alternatives to such involved handling and testing would include:

1) Working with part manufacturers/packagers to obtain parts suitable for testing without special processing (e.g. removable lids, no metal lead frames, etc.)
2) Irradiation at an ultra-high energy heavy-ion facility like the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University where ion beams have sufficient range to penetrate device packaging.

Finally, it is essential to understand that the study of latent damage is still in its infancy and that the state of the art for dealing with this threat to microelectronic part reliability will change as the field matures. Moreover, evolution of microelectronic technology continues to introduce new materials and device structures into state-of the art microelectronics. As such consulting a radiation expert is essential if this risk is to be managed effectively.

Parts Potentially Affected

While high-current failures have been seen in bipolar technologies (e.g. Analog Devices AMP01 instrumentation amplifier), the majority of latent damage concerns arise in CMOS parts that exhibit SEL. In principle, any CMOS part that has not specifically been demonstrated to be immune to SEL (and other high-current error modes) and/or to latent damage should be considered potentially susceptible to both effects. However, of particular concern are parts fabricated on bulk CMOS—such as commercial memories (SRAM, DRAM, FLASH, ferroelectric, etc.), commercial analog-to-digital and digital-to-analog converters (especially high-precision) and so on.

References

1) Becker et al., “Latent Damage in CMOS Devices From Single-Event Latchup,” IEEE Trans. Nucl. Sci., vol. 49, no. 6, p. 3009.
2) Kuboyama et al., “Pseudo and Local SELs Observed in Digital LSIs and Their Implication to SEL Test Method,” accepted for the Nuclear and Space Radiation Effects Conference (NSREC) 2005.

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