

**Magnetospheric Multiscale (MMS) Project**  
***Front-End Electronics Assembly***  
**Specification**  
**DRAFT 5**

**Effective Date: xx/xx/xx**



National Aeronautics and  
Space Administration

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Goddard Space Flight Center  
Greenbelt, Maryland

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1				
2				

## Table of Contents

1.0	Introduction.....	1
1.1	General Information .....	1
1.2	Navigator System.....	1
1.3	Document Scope .....	1
2.0	Applicable Documents.....	2
3.0	Contract Description .....	4
3.1	<i>Front-End Electronics Assembly</i> Description .....	4
4.0	Functional/Performance Requirements .....	5
4.1	<i>FRONT-END ELECTRONICS ASSEMBLY</i> Flight Unit Functional/Performance Requirements .....	5
4.1.1	Operating frequency range .....	5
4.1.2	Gain Characteristics.....	5
4.1.3	Gain Variation (ripple) .....	5
4.1.4	Return Loss .....	5
4.1.5	Noise Figure .....	5
4.1.6	Dynamic Range .....	5
4.1.7	Out of Band Signal Rejection.....	6
4.1.8	Input Rejection Below 1,500 MHz.....	6
4.1.9	Input Rejection Below 1,300 MHz.....	6
4.1.10	Input Rejection Below 999 MHz.....	6
4.1.11	RF Power Survival .....	6
4.1.12	Filter Insertion Loss .....	6
4.1.13	Filter Ripple.....	6
4.1.14	Electrical Interfaces .....	6
4.1.14.1	Input Connector .....	6
4.1.14.1.1	Input Connector Center Conductor .....	7
4.1.14.1.2	Input Connector Shield .....	7
4.1.14.2	Output Connector .....	7
4.1.14.2.1	Output Connector Center Conductor .....	7
4.1.14.2.2	Output Connector Shield.....	7
4.1.14.3	Ground Attach Point on Chassis.....	7
4.2	Resource AllocationS.....	7
4.2.1	Mass Allocation.....	7
4.2.2	Nominal Power Allocation .....	7
4.2.3	Power Goal.....	8
4.3	Power.....	8
4.3.1	Power Input Requirements .....	8
4.3.1.1	Operating Voltage Range.....	8
4.3.1.1	Voltage Ripple .....	8
4.3.1.1	In-rush Current .....	8
4.3.1.1	Sudden Removal of Power.....	8
4.3.1.2	Polarity Reversal Protection .....	8

4.4	Electrical Grounding.....	8
4.4.1	Power DC Isolation .....	8
4.4.1.1	Power DC Isolation from Signal Ground.....	8
4.4.1.2	Power DC Isolation from Component Chassis .....	8
4.4.2	Signal Ground DC Isolation .....	9
4.4.2.1	Input Signal DC Isolation from Output Signal Ground .....	9
4.4.3	Mechanical Contact Impedance.....	9
4.4.4	Mating Method .....	9
4.4.4.1	Multipaction .....	9
4.4.4.2	Corona .....	9
5.0	Physical Requirements.....	10
5.1	Interface Documentation .....	10
5.2	Mass Properties .....	10
5.2.1	RESERVED .....	10
5.2.2	Center of Mass Location .....	10
5.2.3	Center of Mass Accuracy .....	10
5.2.4	Determination of Moments and Products of Inertia.....	10
5.3	Physical Envelope.....	10
5.4	Mounting .....	10
6.0	Environmental Requirements .....	11
6.1	Mechanical Factors of Safety.....	11
6.2	Quasi-Static Acceleration.....	12
6.3	Frequency Requirement.....	12
6.3.1	Fundamental Launch Frequencies .....	12
	RESERVED.....	12
6.3.2	.....	12
6.4	Vibration.....	12
6.4.1	Sinusoidal Vibration .....	12
6.4.2	Random Vibration .....	13
6.5	Shock.....	13
6.6	Acoustics.....	14
6.7	Transportation.....	15
6.8	Pressure.....	15
6.8.1	Operating Pressure Range .....	15
6.8.2	Maximum Depressurization Rate .....	15
6.9	RESERVED .....	15
6.10	Humidity.....	15
6.11	Thermal Requirements .....	15
6.11.1	Flight Interface Design Temperature Limits .....	15
6.11.2	Ground Test Environment.....	16
6.11.3	RESERVED .....	16
6.12	Charge Particle Radiation Requirements .....	16
6.12.1	Definitions .....	16
6.12.2	Total Ionizing Dose .....	18
6.12.2.1	Minimum TID Tolerance for EEE Parts (non-bipolar/bi-CMOS).....	18
6.12.2.2	ELDR Evaluation .....	18

6.12.3	Displacement Damage Dose .....	18
6.12.4	Single Event Effects.....	18
6.12.4.1	Destructive Events (SELs).....	18
6.12.4.2	Non-Destructive Events (SEUs, SETs, SEFIs, SHEs, and MBUs) ...	18
6.12.4.3	Destructive Events (SEBs and SEGRs).....	19
6.12.4.4	MOSFET Derating .....	20
7.0	Cleanliness .....	21
7.1	Surface Contamination .....	21
7.1.1	Surface Contamination Levels At Delivery .....	21
7.1.1.1	Particulate Contamination .....	21
7.1.1.2	Molecular Contamination.....	21
7.1.2	Surface Contamination Generation.....	21
7.1.2.1	Particulate Generation.....	21
7.1.2.2	Molecular Generation .....	22
7.1.2.2.1	Material Selection .....	22
7.1.2.2.2	Assembly Outgassing .....	22
7.2	RESERVED .....	22
7.3	Magnetic Cleanliness.....	22
7.3.1	Minimizing Permanent Fields.....	22
7.3.2	Minimizing Stray Fields .....	23
7.3.2.1	Minimizing Current Loops.....	23
7.3.2.2	Compensating Current Loops .....	24
7.3.2.3	Minimizing Stray Currents .....	24
8.0	Design & Construction requirements .....	25
8.1	Parts, Materials & Processes (PMP).....	25
8.1.1	EEE Parts .....	25
8.1.2	Materials .....	25
8.1.3	RESERVED .....	25
8.2	Electrical .....	25
8.2.1	Test Sensors.....	25
8.2.2	Ground Strap Requirements .....	25
8.2.2.1	Ground Straps, Length to Width Ration.....	25
8.2.2.2	Ground Straps, Material .....	25
8.2.2.3	Ground Lug Contact Area .....	26
8.2.3	RESERVED .....	26
8.2.4	Mitigation of Internal Charging.....	26
8.2.4.1	Mitigation Strategies for Internal Charging .....	26
8.2.4.2	Floating Conductors .....	26
8.2.4.3	Dielectric Structures .....	27
8.2.4.3.1	Bulk Resistivity.....	27
8.2.4.3.2	Charge Bleed-Off.....	27
8.3	Safety.....	27
8.4	Electromagnetic Compatibility .....	27
8.4.1	RESERVED .....	28
8.4.2	RESERVED .....	28
8.4.3	Radiated Emissions .....	28

8.4.3.1	RE01 - Magnetic Field Emissions .....	28
8.4.3.2	RE02 - Electric Field Emissions .....	29
8.4.4	Radiated Susceptibility.....	30
8.4.4.1	RS03 - Electric Field.....	30
	RF Component Unique Tests .....	30
8.4.5	.....	30
8.5	Identification and Marking .....	30
8.6	Workmanship.....	30
8.6.1	Workmanship Standards.....	30
8.6.2	Connector .....	30
8.6.2.1	GSE Cable Connectors .....	30
8.6.2.2	Prevention of Connector Mismatching .....	30
8.6.2.2.1	Connector Uniqueness .....	31
8.6.2.2.2	Connector Facing .....	31
8.6.2.2.3	Connector Keying .....	31
8.6.2.2.4	Accessibility .....	31
8.6.2.2.5	Connector Gender .....	31
8.6.2.3	Test Connectors.....	31
8.6.2.4	Connector Identification.....	31
8.6.2.5	Protection of Unused Test Connectors.....	31
8.6.2.6	Connector Savers.....	31
8.6.3	Safe/Arm Plugs.....	32
8.6.3.1	Safe/Arm Plug Use.....	32
8.6.3.2	Safe/Arm Plugs Connectors .....	32
8.7	Interchangeability.....	32
8.8	Reliability.....	32
8.8.1	Mission Life.....	32
8.8.2	Shelf Life.....	32
9.0	Logistics .....	33
9.1	RESERVED .....	33
9.2	RESERVED .....	33
9.3	RESERVED .....	33
10.0	Verification Requirements .....	34
10.1	Verification Methods .....	34
10.1.1	Inspection .....	34
10.1.2	Analysis .....	34
10.1.3	Test.....	34
10.2	Inspection Requirements .....	34
10.2.1	Visual Inspection.....	34
10.2.2	Physical Measurement.....	35
10.2.3	Documentation Search .....	35
10.3	Analysis Requirements .....	35
10.4	Test Requirements.....	35
10.4.1	Definitions .....	35
10.4.2	Test Factors.....	36
10.4.3	Test Tolerances .....	36

10.4.4	Test Restrictions .....	37
10.4.4.1	Failure During Tests .....	37
10.4.4.2	Modification of Hardware .....	38
10.4.4.3	External Adjustment.....	38
10.4.4.4	Re-Test Requirements.....	38
10.5	Required Tests.....	38
10.5.1	Performance Tests .....	39
10.5.1.1	Comprehensive Performance Test .....	39
10.5.1.2	Functional Test .....	39
10.5.1.3	Abbreviated Functional Test .....	39
10.5.1.4	RESERVED .....	39
10.5.2	Mass Properties Measurement .....	39
10.5.3	Static Loads/Strength Test.....	39
10.5.3.1	Sine Burst .....	40
10.5.3.2	Static Pull.....	40
10.5.4	Sine Sweep Survey .....	40
10.5.5	Sine Vibration .....	41
10.5.6	Random Vibration .....	41
10.5.7	Acoustic Test .....	42
10.5.8	RESERVED .....	42
10.5.9	Shock.....	42
10.5.10	Thermal Bake-out.....	43
10.5.11	Thermal Vacuum Test.....	43
10.5.11.1	Thermal Vacuum Test Parameters.....	43
10.5.11.2	Thermal Vacuum Test Profile .....	43
10.5.12	RESERVED .....	44
10.5.13	Thermal Cycling Testing.....	44
10.5.14	RESERVED .....	45
10.5.15	EMI/EMC Tests .....	45
10.5.15.1	Radiated Emissions Tests .....	45
10.5.15.2	Radiated Susceptibility Tests .....	45
10.5.16	Electrostatic Cleanliness Verification.....	45
10.5.17	Magnetic Tests.....	45
Appendix A	Abbreviations and Acronyms .....	46

## List of Figures

<u>Figure</u>	<u>Page</u>
Figure 3-1 GPS Antenna and Front End Electronics Reference Configuration .....	4
Figure 8-1 Component Level RE01 Radiated Magnetic Field Emission Limits.....	29
Figure 8-2 Component Level RE02 Radiated Electric Field Emission Limits .....	29
Figure 10-1 Thermal Vacuum Profile.....	44

## List of Tables

<u>Table</u>	<u>Page</u>
Table 2-1 Applicable Documents .....	2
Table 6-1 Factors of Safety .....	11
Table 6-2 Front-End Electronics Assembly Limit Loads.....	12
Table 6-3 <i>Front-End Electronics Assembly</i> Sine Vibration Environment.....	13
Table 6-4 <i>Front-End Electronics Assembly</i> Random Vibration Environment.....	13
Table 6-5 Limit Level Shock Response Spectrum.....	14
Table 6-6 Limit Level Acoustic Environments.....	14
Table 6-7 Temperature Levels at Mounting Interface.....	16
Table 6-8 Integral LET Spectrum for Interplanetary Galactic Cosmic Rays (Z=1-92); 100 mils Aluminum Shielding, Values Do Not Include Design Margins .....	19
Table 7-2: Prohibited Magnetic Materials List .....	23
Table 7-3: AC/DC Magnetic Field & Moment Allocation .....	23
Table 8-3 Emission and Susceptibility Requirements.....	28
Table 10-1 Test Factors and Durations .....	36
Table 10-2 Test Tolerances .....	37
Table 10-3 Thermal Vacuum Test Parameters .....	43

## 1.0 INTRODUCTION

### 1.1 GENERAL INFORMATION

The Magnetospheric Multiscale (MMS) mission is the fourth mission of the Solar Terrestrial Probe (STP) program of the National Aeronautics and Space Administration (NASA). The MMS mission will use four identically instrumented observatories to perform the first definitive study of magnetic reconnection in space and will test critical hypotheses about reconnection. Magnetic reconnection is the primary process by which energy is transferred from the solar wind to the Earth's magnetosphere and is also fundamental to the explosive release of energy during substorms and solar flares.

The MMS mission will study magnetic reconnection in the Earth's magnetosphere. The four MMS observatories will be required to fly in a tetrahedral formation in order to unambiguously determine the orientation of the magnetic reconnection layer.

The four satellites are spin-stabilized and flown in a tightly controlled formation through a highly elliptical Earth orbit. S-Band RF communications will be supported using the 34m DSN, 13m USN and TDRSS networks.

Each satellite has its spin axis oriented roughly normal to the ecliptic plane. Each satellite will be equipped with two S-Band communication antennas each mounted slightly above the top and bottom panel's surfaces.

Integral to the MMS Mission and spacecraft operation is the Navigator Subsystem that provides onboard navigation functions. Navigator uses the Global Position Satellite system to purpose is to provide spacecraft location data.

### 1.2 NAVIGATOR SYSTEM

MMS Navigator subsystem consists of a receiver/processor unit fed by four functionally identical receive channels. On orbit, the Navigator subsystem uses GPS information to perform orbit determination calculations. Each receive channel of the GPS subsystem will incorporate a sector antenna, and a Front-End Electronics Assembly. During the mission the spacecraft will be below and well above the GPS constellation. The Front-End Electronics Assemblies are integral to the subsystems weak signal performance.

### 1.3 DOCUMENT SCOPE

This specification describes the electrical, mechanical, environmental, and verification testing requirements for a space-qualified *Front-End Electronics Assembly* (FEA) for a Goddard Space Flight Center (GSFC) payload, the Magnetospheric Multiscale (MMS) Mission.

## 2.0 APPLICABLE DOCUMENTS

The following documents and drawings in effect on the day this specification was signed **shall** apply to the fabrication and to the electrical, mechanical, and environmental requirements of the *Front-End Electronics Assembly* to the extent specified herein. In the event of conflict between this specification and any referenced document, this specification will govern, with the exception of the Magnetospheric Multiscale *Front-End Electronics Assembly* Statement of Work (461-NAV-SOW-0021), in which case the Statement of Work (SOW) takes precedence.

The following is a list of the applicable specifications and publications.

**Table 2-1 Applicable Documents**

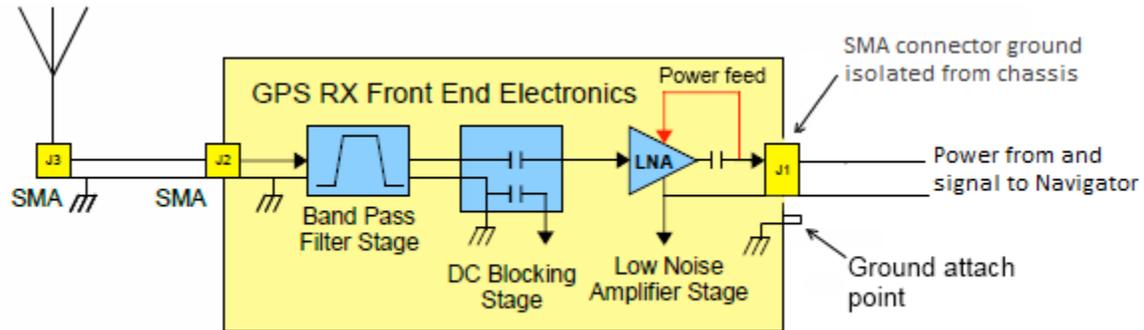
Section	Document Number	Title	Revision/Date
Many	461-NAV-SOW-0021	MMS <i>Front-End Electronics Assembly</i> Statement of Work	<i>TBD</i>
Many	461-NAV-LIST-0035	MMS <i>Front-End Electronics Assembly</i> DILS	<i>TBD</i>
1.1.1.1	ANSI/TIA/EIA-422-B	Electrical Characteristics of Balanced Voltage Digital Interface Circuits	09/16/2005
1.1.1.1	ANSI/TIA/EIA-644-A-2001	Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits	02/2001
1.0	MIL-STD-1576	Electroexplosive Subsystem Safety Requirements and Test Methods for Space Systems	07/31/1984
6.1	NASA-STD-5001A	Structural Design And Test Factors Of Safety For Spaceflight Hardware	08/05/2008
6.1 10.5.8	AFSPCMAN 91-710	Range Safety User Requirements	07/01/2004
1.1.1	NASA-HDBK-7005	Dynamic Environment Criteria	BASE/ 3/13/2001
1.1.1	NASA-STD-7001	Payload Vibroacoustic Test Criteria	BASE/ 6/21/1996
7.1.1.2	IEST-STD-CC1246D	Product Cleanliness Levels And Contamination Control Program	2002
7.1.2.2.1	ASTM E-595-07	Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment	12/01/2007
8.1.2	MIL-DTL-5541	Chemical Conversion Coatings on Aluminum and Aluminum Alloys	07/11/2006
8.1.2	AMS 2488	Anodic Treatment - Titanium and Titanium Alloys Solution Ph 13 Or Higher	06/01/2000
8.1.2	MIL-A-8625F(1)	Anodic Coatings for Aluminum and Aluminum Alloys	09/15/2003
0 0 0 0	EEE-INST-002	Instructions for EEE Parts Selection, Screening, Qualification, and Derating	04/2008

<b>Section</b>	<b>Document Number</b>	<b>Title</b>	<b>Revision/Date</b>
0	DOD-HDBK-83575	General Handbook for Space Vehicle Wiring Harness Design and Testing	06/04/1998
0	NASA-STD-8739.3	Requirements for Soldered Electrical Connections	12/15/97
0	NASA-STD-8739.4	Requirements for Crimping Inter-connecting Cables, Harnesses, and Wiring	02/09/98
8.4	MIL-STD-461C	Military Standard, Electromagnetic Emission And Susceptibility Requirements For The Control Of Electromagnetic Interference (Emi)	08/04/1986

### 3.0 CONTRACT DESCRIPTION

#### 3.1 FRONT-END ELECTRONICS ASSEMBLY DESCRIPTION

The *Front-End Electronics Assembly* (FEA) is an RF electronics device that is capable of filtering and amplifying the incoming GPS signals from an antenna and delivering the signal to the Navigator subsystem.



**Figure 3-1 GPS Antenna and Front End Electronics Reference Configuration**

In Figure 3-1 a notional architecture is shown to illustrate the functionality of the Front-End Electronics Assembly. It is anticipated that the assembly will comprise a DC block, receive band-pass filter (BPF) and a Low Noise Amplifier (LNA). The order of components shown in the Figure should not be interpreted to impose a specific implementation, except for the orientation of the DC block before the LNA. Other configurations are acceptable if overall requirements are met. A critical design component of the Front-End Electronics Assembly is the output connector, which is described in section 4.2.2. The Front-End Electronics Assembly is intended to be powered via the RF output interface. The power must be isolated from the chassis.

## 4.0 FUNCTIONAL/PERFORMANCE REQUIREMENTS

The component **shall** be designed to withstand the operational and non-operational environments specified in the following section without degradation to mission goals and performance requirements.

### 4.1 FRONT-END ELECTRONICS ASSEMBLY FLIGHT UNIT FUNCTIONAL/PERFORMANCE REQUIREMENTS

For the GPS Front-End Electronics Assembly, the operating frequency range (OFR) is defined as the frequency between 1574.32 MHz to 1576.52 MHz. This definition is relevant for the gain characteristics, but should not necessarily dictate the specifications of the filter within the Front-End Electronics Assembly.

#### 4.1.1 Operating frequency range

The GPS Front-End Electronics Assembly **shall** have an operating frequency range (OFR) from 1574.32 MHz to 1576.52 MHz. The 3dB bandwidth of the filter does not need to match the OFR as long as it meets the other limiting frequency characteristics.

#### 4.1.2 Gain Characteristics

The GPS Front-End Electronics Assembly output **shall** have a minimum gain of 40 dB in the operating frequency range.

#### 4.1.3 Gain Variation (ripple)

The GPS Front-End Electronics Assembly **shall** have a ripple in gain of less than 0.2 dB over the operating frequency range.

#### 4.1.4 Gain Stability

The GPS Front-End Electronics Assembly **shall** have gain stability up to 5:1 load pull.

#### 4.1.5 Return Loss

The GPS Front-End Electronics Assembly **shall** have an input and output return loss of greater than 15 dB, with reference to 50 ohms.

#### 4.1.6 Noise Figure

The GPS Front-End Electronics Assembly output **shall** have a noise figure < 1.5 dB.

#### 4.1.7 Dynamic Range

The GPS Front-End Electronics Assembly **shall** have a 1 dB compression point > 12 dBm at the output.

#### 4.1.8 Out of Band Signal Rejection

The GPS Front-End Electronics Assembly **shall** reject input signals which are above 2,100 MHz by a minimum of 70 dB attenuation. The term reject is defined as firstly the relative attenuation of the signal level at the output to protect downstream receiver dynamic range, and secondly to protect LNA dynamic range.

#### 4.1.9 Input Rejection Below 1,500 MHz

The GPS Front-End Electronics Assembly **shall** reject input signals which are below 1,500 MHz by a minimum of 30 dB attenuation.

#### 4.1.10 Input Rejection Below 1,300 MHz

The GPS Front-End Electronics Assembly **shall** reject input signals which are below 1,300 MHz by a minimum of 50 dB attenuation.

#### 4.1.11 Input Rejection Below 999 MHz

The GPS Front-End Electronics Assembly **shall** reject input signals which are below 999 MHz by a minimum of 70 dB attenuation.

#### 4.1.12 RF Power Survival

The GPS Front-End Electronics Assembly **shall** survive without damage an input maximum RF power level of -10 dBm with a goal of 0 dBm or greater while powered on.

#### 4.1.13 Filter Insertion Loss

The band pass filter **shall** have an insertion loss of less than 0.75 dB over the operating frequency range.

#### 4.1.14 Filter Ripple

The band pass filter **shall** have a ripple in insertion loss over the operating frequency range of under 0.1 dB.

### 4.2 ELECTRICAL INTERFACES

#### 4.2.1 Input Connector

The input connector **shall** be a female SMA which will be connected to the GPS antenna.

#### 4.2.1.1 Input Connector Center Conductor

The input connector SMA center conductor **shall** be used as the RF signal input.

#### 4.2.1.2 Input Connector Shield

The input connector SMA shield **shall** be tied to chassis with a  $<2.5 \text{ m}\Omega$  DC resistance.

#### 4.2.1.3 Input Connector Impedance

The RF input impedance **shall** be  $50 \Omega \pm \text{TBD}$  over the operating frequency. The antenna has a  $50 \Omega$  impedance.

### 4.2.2 Output Connector

The output connector **shall** be a female SMA, isolated from chassis. The connector is used for power input and RF output.

#### 4.2.2.1 Output Connector Center Conductor

The output connector SMA center conductor **shall** be used as power input and RF signal output.

#### 4.2.2.2 Output Connector Shield

The output connector SMA shield **shall** be used as power return and signal return.

#### 4.2.2.3 Input Connector Impedance

The RF output impedance **shall** be  $50 \Omega \pm \text{TBD}$  over the operating frequency. .

### 4.2.3 Ground Attach Point on Chassis

A chassis ground attachment point **shall** be provided near the output connector.

## 4.3 RESOURCE ALLOCATIONS

### 4.3.1 Mass Allocation

The *Front-End Electronics Assembly* **shall** have a mass of less than or equal to 650 grams each.

### 4.3.2 Nominal Power Allocation

The *Front-End Electronics Assembly* **shall** have a nominal (continuous) power consumption of less than or equal to 350 mW.

### 4.3.3 Power Goal

The GPS Front-End Electronics Assembly power dissipation should not exceed 330mW.

## 4.4 POWER

### 4.4.1 Power Input Requirements

#### 4.4.1.1 Operating Voltage Range

The *Front-End Electronics Assembly* **shall** be designed to operate over the voltage range of +4.6V to +5.2 VDC at their primary power inputs.

#### 4.4.1.2 Voltage Ripple

The *Front-End Electronics Assembly* **shall** be designed to meet its performance requirements in the presence of ripple voltages up to 60 mVp-p.

#### 4.4.1.3 In-rush Current

The *Front-End Electronics Assembly* **shall** be designed to have an in-rush current of <750 mA per unit upon application of power.

#### 4.4.1.4 Sudden Removal of Power

The *Front-End Electronics Assembly* **shall** meet its performance requirements without degradation after exposure to an abrupt, unannounced removal of power.

#### 4.4.1.5 Polarity Reversal Protection

The *Front-End Electronics Assembly* should have built-in protection to prevent damage due to polarity reversal at the power inputs, where feasible.

## 4.5 ELECTRICAL GROUNDING

### 4.5.1 Power DC Isolation

#### 4.5.1.1 Power DC Isolation from Signal Ground

The *Front-End Electronics Assembly* power and power returns **shall** be isolated from input signal grounds by a DC resistance of greater than or equal to 10 MΩ.

#### 4.5.1.2 Power DC Isolation from Component Chassis

The *Front-End Electronics Assembly* power and power returns **shall** be isolated from the component chassis by a DC resistance of greater than or equal to 10 MΩ.

## 4.5.2 Signal Ground DC Isolation

### 4.5.2.1 Input Signal DC Isolation from Output Signal Ground

The *Front-End Electronics Assembly* input signal ground **shall** be isolated from output signal grounds by a DC resistance of greater than or equal to 10 MΩ.

## 4.5.3 Mechanical Contact Impedance

The DC resistance of the mechanical contact between two conductive mating surfaces (internal to the component, and at the spacecraft interface) **shall** be less than or equal to 2.5 mΩ DC resistance.

## 4.5.4 Mating Method

The primary mating method for a component **shall** be metal-to-metal contact between component mounting feet (or base plate) and the spacecraft structure.

### 4.5.4.1 Multipaction

All RF components **shall** be designed to preclude damage or measurable degradation in performance due to multipaction while operating in a vacuum environment.

### 4.5.4.2 Corona

RF components that must operate during the launch and ascent stages **shall** be designed to preclude damage or measurable degradation in performance due to corona.

## 5.0 PHYSICAL REQUIREMENTS

### 5.1 INTERFACE DOCUMENTATION

The mounting interface **shall** be defined in the Mechanical Interface Control Drawing (ICD), which will be developed between the contractor and NASA GSFC.

The electrical interface **shall** be defined in the Electrical Interface Control Drawing (ICD), which will be developed between the contractor and NASA GSFC.

The data interface **shall** be defined in the Data Interface Control Drawing (ICD), which will be developed between the contractor and NASA GSFC.

### 5.2 MASS PROPERTIES

#### 5.2.1 RESERVED

#### 5.2.2 Center of Mass Location

The contractor **shall** define the center of mass.

#### 5.2.3 Center of Mass Accuracy

The center of mass **shall** be determined to within  $\pm 2.5 \text{ mm}$  relative to an external reference.

#### 5.2.4 Determination of Moments and Products of Inertia

The final moments and products of inertia of *Front-End Electronics Assembly* **shall** be calculated.

### 5.3 PHYSICAL ENVELOPE

The *Front-End Electronics Assembly* **shall** not exceed the thermal and mechanical volume envelope of 15 cm length X 8 cm width X 3.5 cm height.

### 5.4 MOUNTING

The mounting of the Front-End Electronics Assembly shall be determined by an ICD as specified in Section 5.1

## 6.0 ENVIRONMENTAL REQUIREMENTS

Environmental design requirements for the spacecraft components are specified in this section. The MMS spacecraft components will be capable of meeting their performance requirements after exposure to the environments specified in this section.

All loads and environments in this document are preliminary and will be updated as the MMS spacecraft is defined.

### 6.1 MECHANICAL FACTORS OF SAFETY

The *Front-End Electronics Assembly* as well as Mechanical Ground Support Equipment (MGSE) **shall** demonstrate positive Margins of Safety under limit loads for all yield and ultimate failures using the Factors of Safety (FS) defined in Table 6-1 (see NASA-STD-5001A for more information on other materials [e.g. glass]). Margin of Safety (MS) is defined as follows:

$$MS = (\text{Allowable Stress(or Load)} / (\text{Applied Limit Stress(or Load)} \times FS)) - 1$$

**Table 6-1 Factors of Safety**

Type of Hardware <sup>1,2</sup>	Static/Sine	Random/Acoustic <sup>4</sup>
Tested Metallic Structure Yield	1.25	1.6
Tested Metallic Structure Ultimate	1.4	1.8
Stability Ultimate	1.4	1.8
Beryllium Yield	1.4	1.8
Beryllium Ultimate	1.6	2.0
Composite Ultimate <sup>3</sup>	1.5	1.9
Bonded Inserts/Joints Ultimate	1.5	1.9
Untested Flight Structure Yield- metallic only	2.0	
Untested Flight Structure Ultimate - metallic only	2.6	
Ground Support Equipment Yield	3.0	
Ground Support Equipment Ultimate	5.0	
Transportation Dolly/Shipping Container Yield	2.0	
Transportation Dolly/Shipping Container Ultimate	3.0	

1 – Factors of safety for pressurized systems to be compliant with AFSPCMAN 91-710, “Range Safety User Requirements.”

2 – Factors of safety for glass and structural glass bonds specified in NASA-STD-5001.

3 – All composite structures must be tested to 1.25 x limit loads.

4 – Factors shown should be applied to statistically derived peak response based on RMS level. As a minimum, the peak response **shall** be calculated as a 3-sigma value.

## 6.2 QUASI-STATIC ACCELERATION

Quasi-static acceleration represents the combination of steady-state accelerations and the low frequency mechanically transmitted dynamic accelerations that occur during launch.

The *Front-End Electronics Assembly* **shall** demonstrate its ability to meet its performance requirements after being subjected to the net CG limit loads shown in Table 6-2.

Linear interpolation should be used between breakpoints to determine the appropriate limit load as a function of *Front-End Electronics Assembly* weight. Note that these design limit loads are intended to cover only the low frequency launch environment and must be used in conjunction with the random vibration environments to assess structural margins.

**Table 6-2 Front-End Electronics Assembly Limit Loads**

<i>Front-End Electronics Assembly Mass (kg)</i>	<b>Limit Load (g, any direction)</b>
0.5 or less	35.9
1	35.0

## 6.3 FREQUENCY REQUIREMENT

### 6.3.1 Fundamental Launch Frequencies

The *Front-End Electronics Assembly* **shall** have a fundamental frequency greater than 75 Hz when hard mounted at its SC interface.

### 6.3.2 RESERVED

## 6.4 VIBRATION

### 6.4.1 Sinusoidal Vibration

The *Front-End Electronics Assembly* **shall** demonstrate its ability to meet its performance requirements after being subjected to the sine vibration environment in Table 6-3, applied at the MMS to *Front-End Electronics Assembly* interface. See Section 10.4.1 for definitions of Protoflight, Qual, and Acceptance.

**Table 6-3 Front-End Electronics Assembly Sine Vibration Environment**

Frequency	Protoflight/Qual Level	Acceptance Level
5 - 50 Hz	12.5 g <sup>2</sup> s (4 oct/min protoflight and 2 oct/min prototype hardware)	10 g <sup>2</sup> s (4 oct/min)

Levels may be notched to not exceed 1.25 times the design limit load. These levels will be updated as coupled-loads analysis (CLA) data becomes available. *Front-End Electronics Assembly* **shall** test for this environment up to 50 Hz and be analyzed from 50 to 100 Hz. Peak levels at the low end of the frequency range (5 – 20 Hz typically) may be ramped up as needed to accommodate shaker table displacement limitations.

#### 6.4.2 Random Vibration

The *Front-End Electronics Assembly* **shall** demonstrate its ability to meet its performance requirements after being subjected to the random vibration environment in Table 6-4, applied at the MMS to *Front-End Electronics Assembly* interface.

**Table 6-4 Front-End Electronics Assembly Random Vibration Environment**

Frequency (Hz)	Protoflight/Qual Level	Acceptance Level
20	0.026 g <sup>2</sup> /Hz	0.013 g <sup>2</sup> /Hz
20 – 50	+6 dB/Octave	+6 dB/Octave
50 – 800	0.160 g <sup>2</sup> /Hz	0.080 g <sup>2</sup> /Hz
800 – 2000	-6 dB/Octave	-6 dB/Octave
2000	0.026 g <sup>2</sup> /Hz	0.013 g <sup>2</sup> /Hz
Over All	14.1 grms	10.0 grms
Duration (minutes)	1 (protoflight), 2 (Qual)	1

The above random environment is appropriate for *Front-End Electronics Assembly* weighing 22.7 kg (50 lbs) or less. This environment will be updated with random vibration analysis. Note for lightweight *Front-End Electronics Assembly*, the highest design loads may be from this random vibration environment. The contractor **shall** perform random vibration analysis along with static loads analysis. Please see NASA-HDBK-7005 and NASA-STD-7001 for more information.

#### 6.5 SHOCK

The GPS Front-End Electronics Assembly shall be designed to meet its performance requirements after being subjected to the shock environment in Table 6-5, applied at the GPS Front-End Electronics Assembly interface.

**Table 6-5 Limit Level Shock Response Spectrum**

Frequency (Hz)	AcceptanceLevel (Q=10)	Protoflight Level
100	36 g	51 g
100 to 440	9.9 dB/Octave	9.9 dB/Octave
440 to 500	407 g	573 g
500 to 557	9.9 dB/Octave	9.9 dB/Octave
557 to 10000	481 g	678 g
Three Mutually Perpendicular Axes		

## 6.6 ACOUSTICS

The *Front-End Electronics Assembly* **shall** be designed to meet its performance requirements after being subjected to the acoustic environment listed in Table 6-6.

**Table 6-6 Limit Level Acoustic Environments**

Center Frequency (Hz)	Max Predicted Sound Pressure Level (dB)
25	114.0
31.5	120.3
40	127.5
50	122.5
63	124.0
80	124.5
100	126.0
125	126.0
160	127.1
200	127.0
250	126.5
315	126.0
400	126.0
500	124.5
630	122.0
800	119.5
1000	116.5
1250	114.0
1600	112.0
2000	114.0
2500	111.0
3150	110.0
4000	109.0
5000	108.5
6300	108.0
8000	109.7

Center Frequency (Hz)	Max Predicted Sound Pressure Level (dB)
10000	110.5
OASPL	137.1
Duration	1 minute flight and 2 minutes non-flight hardware

The reference point is 20  $\mu$ Pa.

## 6.7 TRANSPORTATION

All Transportation loads that the *Front-End Electronics Assembly* is exposed to **shall** be less than the Quasi-Static, Vibration, Shock, and Acoustic loads previously defined.

## 6.8 PRESSURE

### 6.8.1 Operating Pressure Range

The *Front-End Electronics Assembly* **shall** be designed to meet all performance requirements while operating over a pressure range of  $1.08 \times 10^5$  N/m<sup>2</sup> (813 Torr) to  $1.3 \times 10^{-12}$  N/m<sup>2</sup> ( $1 \times 10^{-14}$  Torr).

### 6.8.2 Maximum Depressurization Rate

The *Front-End Electronics Assembly* **shall** be designed to meet all performance requirements after exposure to a maximum depressurization rate of 6205.3 N/m<sup>2</sup>/second (46.54 Torr/sec) experienced during launch and ascent.

## 6.9 RESERVED

## 6.10 HUMIDITY

The *Front-End Electronics Assembly* **shall** be able to meet performance requirements after exposure to relative humidity levels of 35% to 70%.

## 6.11 THERMAL REQUIREMENTS

### 6.11.1 Flight Interface Design Temperature Limits

When powered "OFF", the *Front-End Electronics Assembly* **shall** be capable of surviving indefinitely when its temperatures are within the survival limits shown in Table 6-7 without damage or permanent performance degradation.

The *Front-End Electronics Assembly* **shall** also survive indefinitely, without damage or permanent performance degradation, if powered "ON" anywhere within the Operational and Protoflight/Acceptance limits shown in Table 6-7.

The *Front-End Electronics Assembly* **shall** demonstrate turn on at the cold Operational (out of spec) limit shown in Table 6-7.

**Table 6-7 Temperature Levels at Mounting Interface**

	Minimum Temperature (°C)	Maximum Temperature (°C)
Operational (In Spec)	-15	+40
Operational (Out of Spec)	-20	+45
Protoflight/Acceptance (In Spec)	-25	+60
Survival (Unpowered)	-25	+60

### 6.11.2 Ground Test Environment

The *Front-End Electronics Assembly* **shall** be able to operate in a lab environment with air temperature between 15 and 25 degrees C and relative humidity between 35 and 70%.

The *Front-End Electronics Assembly* **shall** survive without degradation during transportation temperatures of +15 to +30 degrees C and relative humidity of 0 to 70%.

### 6.11.3 RESERVED

## 6.12 CHARGE PARTICLE RADIATION REQUIREMENTS

S/C procured components containing electronic parts will be exposed to a natural space radiation environment that consists of: (1) trapped particles which include electrons, protons, and heavier ions; (2) particles from solar events (coronal mass ejections and flares); and (3) galactic cosmic ray particles.

### 6.12.1 Definitions

*Total Ionizing Dose (TID)* - the mean energy deposited by ionizing radiation in a device region divided by the mass of the region. This is often given in units of rad(Si), where 1 rad(Si) = 100 erg deposited per gram of silicon.

*Displacement Damage Dose (DDD)* - the mean energy deposited by ionizing radiation in a device region that goes into atomic displacements divided by the mass of the region. There is no official unit for DDD. One such unit is MeV/g

*Single Event Effect (SEE)* - any measurable effect to a circuit due to an ion strike. This includes, but is not limited to, single event upsets (SEUs), single event transients (SETs), single hard errors (SHEs), single event latchups (SELs), single event functional interrupts (SEFIs), single event burnouts (SEBs), single event gate ruptures (SEGRs), and single event dielectric ruptures (SEDRs).

*Single Event Upset (SEU)* - a change of state or transient induced by an energetic particle such as a cosmic ray or proton in a device. This may occur in digital or analog, circuits and may have effects in surrounding interface circuitry (a subset known as SETs). These are “soft” errors in that a reset or rewriting of the device will usually return the device to normal behavior thereafter. The general goal for non-destructive events such as SEUs or SETs is not to avoid them completely, but to manage their impact through robust circuit design, automatic correction, and/or operational activities based on knowledge from ground radiation tests and circuit/system analysis.

*Single Hard Error (SHE)* - a SEU that causes a permanent change to the operation of a device. An example is a stuck bit in a memory device.

*Multiple Bit Upset (MBU)* - an event induced by a single energetic particle such as a cosmic ray or proton that causes multiple upsets or transients during its path through a device or system in a single logical structure (ex., 2 bits affected in a single 16-bit word).

*Single Event Functional Interrupt (SEFI)* - a condition that causes loss of device functionality due to a single event in a control portion of a device. It generally requires a device reset or a re-initialization to resume normal device operations, but, for some devices, a power cycle is necessary to resume normal device operations. The general goal for non-destructive events such as SEFI is to avoid them, however, managing their impact through robust circuit design, automatic correction, and/or operational activities may be considered.

*Single Event Latchup (SEL)* - a condition that may cause device failure due to a single event induced high current state. A SEL may or may not cause permanent device damage, but requires power cycling of the device to resume normal device operations. In addition, susceptible devices have the concern for latent damage (device does not fail from the immediate single particle event, but reliability is degraded and premature failure may occur).

*Single Event Burnout (SEB)* - a condition that can cause device destruction due to a high current state in a power transistor.

*Single Event Gate Rupture (SEGR)* - a single ion induced condition in power MOSFETs that may result in the formation of a conducting path in the gate oxide.

*Linear Energy Transfer (LET)* - a measure of the energy deposited per unit length as an energetic particle travels through a material. The common LET unit is MeV\*cm<sup>2</sup>/milligram (mg) of material.

*Threshold LET (LET<sub>th</sub>)* - the maximum LET at which no SEE is observed at a particle fluence of 10<sup>7</sup> ions/cm<sup>2</sup>.

*Non-Ionizing Energy Loss (NIEL)* - a measure of the rate of energy loss due to atomic displacements as a particle traverses a material..

## 6.12.2 Total Ionizing Dose

### 6.12.2.1 Minimum TID Tolerance for EEE Parts (non-bipolar/bi-CMOS)

All EEE parts (except bipolar/bi-CMOS) **shall** be able to tolerate two times (x2) the dose shown for the TID curves in , assuming 1.016mm of aluminum S/C shielding, plus the contractor specific box shielding.

### 6.12.2.2 ELDR Evaluation

All parts based on bipolar or bi-CMOS technology that are susceptible to Enhanced Low Dose Rate (ELDR) effects shall show that no dose rate enhancement effects exist for seven times (x7) the dose shown on the TID curve, assuming 1.016 mm of aluminum S/C shielding for items protected by the decks/solar arrays, plus the vendor specific box shielding.

## 6.12.3 Displacement Damage Dose

All DDD susceptible EEE parts shall not sustain permanent damage or performance degradation due to a minimum 10 MeV equivalent proton fluence of  $3.4 \times 10^{11} \text{ cm}^{-2}$ .

## 6.12.4 Single Event Effects

### 6.12.4.1 Destructive Events (SELs)

All EEE parts shall be immune to destructive SELs, up to an LET threshold of  $75 \text{ MeV-cm}^2/\text{mg}$ .

### 6.12.4.2 Non-Destructive Events (SEUs, SETs, SEFIs, SHEs, and MBUs)

All EEE parts with an SEE LET threshold of  $< 75 \text{ MeV-cm}^2/\text{mg}$  shall have less than 1 critical effect (requires external intervention to correct) in 50 years, using the LET fluences in Table 6-8.

**Table 6-8 Integral LET Spectrum for Interplanetary Galactic Cosmic Rays (Z=1-92); 100 mils Aluminum Shielding, Values Do Not Include Design Margins**

LET (MeV*sqcm/mg)	LET Fluence (#/sqcm/day)	LET Fluence (#/sqcm/day)	LET (MeV*sqcm/mg)	LET Fluence (#/sqcm/day)	LET Fluence (#/sqcm/day)
	Solar Minimum	Solar Maximum		Solar Minimum	Solar Maximum
1.00E-03	4.25E+05	1.54E+05	2.01E+00	3.39E+01	5.88E+00
1.65E-03	4.24E+05	1.54E+05	3.02E+00	1.43E+01	2.03E+00
1.69E-03	3.29E+05	1.07E+05	3.99E+00	7.76E+00	1.02E+00
1.70E-03	3.04E+05	9.42E+04	5.03E+00	4.59E+00	5.81E-01
1.72E-03	2.84E+05	8.46E+04	5.99E+00	3.07E+00	3.80E-01
1.77E-03	2.54E+05	7.02E+04	8.00E+00	1.55E+00	1.90E-01
1.81E-03	2.30E+05	5.98E+04	1.01E+01	9.00E-01	1.10E-01
1.85E-03	2.12E+05	5.20E+04	1.11E+01	7.17E-01	8.75E-02
1.91E-03	1.90E+05	4.34E+04	1.20E+01	5.76E-01	7.04E-02
1.98E-03	1.72E+05	3.75E+04	1.30E+01	4.67E-01	5.71E-02
2.01E-03	1.67E+05	3.59E+04	1.40E+01	3.85E-01	4.72E-02
2.13E-03	1.46E+05	3.05E+04	1.50E+01	3.16E-01	3.88E-02
2.28E-03	1.27E+05	2.69E+04	1.60E+01	2.61E-01	3.20E-02
2.53E-03	1.07E+05	2.39E+04	1.70E+01	2.20E-01	2.71E-02
3.01E-03	8.29E+04	2.11E+04	1.80E+01	1.85E-01	2.27E-02
3.54E-03	6.87E+04	1.98E+04	1.91E+01	1.54E-01	1.89E-02
4.52E-03	5.55E+04	1.88E+04	2.00E+01	1.30E-01	1.60E-02
5.56E-03	4.90E+04	1.83E+04	2.49E+01	4.45E-02	5.50E-03
6.54E-03	4.58E+04	1.82E+04	3.00E+01	6.27E-04	8.18E-05
7.52E-03	2.76E+04	7.46E+03	3.49E+01	6.86E-05	1.06E-05
8.55E-03	2.13E+04	5.04E+03	4.01E+01	4.18E-05	6.50E-06
9.60E-03	1.75E+04	3.97E+03	4.50E+01	2.83E-05	4.42E-06
1.97E-02	7.02E+03	1.88E+03	5.00E+01	2.00E-05	3.13E-06
2.96E-02	5.07E+03	1.63E+03	5.06E+01	1.92E-05	3.00E-06
4.00E-02	4.33E+03	1.55E+03	5.55E+01	1.34E-05	2.11E-06
5.04E-02	3.81E+03	1.43E+03	6.02E+01	9.38E-06	1.49E-06
6.00E-02	3.50E+03	1.36E+03	6.53E+01	6.32E-06	1.01E-06
6.97E-02	2.91E+03	1.08E+03	7.00E+01	4.40E-06	7.01E-07
8.01E-02	2.66E+03	1.01E+03	7.50E+01	2.83E-06	4.52E-07
9.00E-02	2.40E+03	9.12E+02	8.04E+01	1.65E-06	2.63E-07
1.01E-01	2.23E+03	8.74E+02	8.52E+01	7.71E-07	1.23E-07
2.00E-01	9.84E+02	3.59E+02	9.03E+01	1.94E-07	3.10E-08
4.02E-01	4.33E+02	1.52E+02	9.57E+01	2.88E-08	4.60E-09
6.03E-01	2.90E+02	1.10E+02	1.00E+02	1.19E-08	1.89E-09
7.96E-01	2.23E+02	8.84E+01	1.01E+02	5.27E-09	8.41E-10
1.00E+00	1.79E+02	7.22E+01	1.03E+02	2.54E-09	4.05E-10

**6.12.4.3 Destructive Events (SEBs and SEGRs)**

In components containing power LET transistors, all power transistors shall have a SEGR and SEB threshold LET > 75 MeV-cm<sup>2</sup>/mg when biased at 133% of the application V<sub>ds</sub> or V<sub>ce</sub>.

#### **6.12.4.4 MOSFET Derating**

MOSFETs that are operated in the linear region shall be derated to 75% of the highest passing  $V_{ds}$ .

## 7.0 CLEANLINESS

At delivery, the *Front-End Electronics Assembly* should be sufficiently clean so as not to adversely affect its own performance, as well as not be a source of contamination to other items. In addition, the *Front-End Electronics Assembly* should not generate contaminants following delivery in excess of that permitted below by virtue of its design, materials of construction, or operation.

### 7.1 SURFACE CONTAMINATION

#### 7.1.1 Surface Contamination Levels At Delivery

##### 7.1.1.1 Particulate Contamination

The *Front-End Electronics Assembly* **shall** be free of particulate and molecular contamination when inspected with a bright and white light in a darkened room.

##### 7.1.1.2 Molecular Contamination

The *Front-End Electronics Assembly* **shall** meet a molecular surface cleanliness level of A/3 per IEST-STD-1246D on all external and critical surfaces, when tested in accordance with IEST-STD-1246D.

#### 7.1.2 Surface Contamination Generation

##### 7.1.2.1 Particulate Generation

The *Front-End Electronics Assembly* contractor **shall** not employ any of the following particle generating materials or processes into the *Front-End Electronics Assembly* design or construction without prior approval from NASA/GSFC:

- Paints prone to shedding due to large paint pigment molecules, overspray, poor adhesion, etc.
- Dry lubricants (e.g. molybdenum disulfide).
- Surfaces prone to corrosion or oxides because of a lack of corrosion protection or dissimilar metals in close contact.
- Fabrics with brittle constituents (e.g., composites, graphite or glass).
- Perforated materials when material is highly susceptible to tear propagation (e.g., MLI).
- Metal oxides (bare [untreated] aluminum and magnesium, iron, non-corrosion resistant steel, etc.).
- Braided metallic or synthetic wires, ropes, slings, etc. unless measures have been taken to contain any broken filaments or fibers (sheathing, sealing with polymers, covering, etc.).
- Woven materials especially cut or unfinished ends (metal braid, EMI shielding, lacing cord, expando sleeving), unless measures have been taken to prevent

fraying or generation of particles (cut with a hot knife, seal with polymer, bag, etc).

- Materials with thin films known to erode or crack or flake when subjected to normal handling (e.g., indium tin oxide [ITO] or other rigid or brittle semiconductor or ceramic coating on flexible substrates, Teflon, multi-layered insulation [MLI], etc.).
- Foams, highly textured materials.
- Trapped debris in holes.

### 7.1.2.2 Molecular Generation

#### 7.1.2.2.1 Material Selection

The *Front-End Electronics Assembly* materials **shall** have a total mass loss (TML) less than 1.00% and a collected volatile condensable mass (CVCM) less than 0.10%, as specified in ASTM E-595 unless a materials usage agreement has been generated and approved by NASA/GSFC. Silicones should be avoided or minimized. It is highly recommended that silicones be baked out at a high temperature prior to integration into the system to prevent extended bakeouts of the entire assembly.

#### 7.1.2.2.2 Assembly Outgassing

When measured in a vacuum of 10E-6 torr at 50 °C, the *Front-End Electronics Assembly* outgassing **shall** not exceed 2E-10 g/sec per kg of unit under test of mass that is condensable on a Quartz Crystal Monitor (QCM) that is operated at -20 degrees.

## 7.2 RESERVED

## 7.3 MAGNETIC CLEANLINESS

To avoid corrupting the magnetic measurements that are a prime objective of the mission, the observatory and its subsystems are required to be “magnetically clean.” The following paragraphs provide requirements and guidelines for minimizing the magnetic field generated by the observatory.

### 7.3.1 Minimizing Permanent Fields

Permanent fields arise from permanent magnets or magnetically soft materials that are magnetized in response to varying electrical or magnetic fields in ambient environment. Permanent fields should be minimized by: (a) strictly controlling the use of magnetic materials and (b) compensating the permanent fields.

The material described in Table 7-1 **shall** be prohibited from Observatory. Exceptions to this requirement can be made case by case upon completion of the magnetic assessment and the MMS project office approval

**Table 7-1: Prohibited Magnetic Materials List**

Alloy 426	Mumetal
Alloy 720 <sup>1</sup>	Nichrome
Carbon Steel 1008	Nickel 200, 270
Chromium	Nickel Iron
Cobalt	Pelcoloy
Copperweld	Permalloy
Dumet	Platinum
Electroless Nickel (except high-phosphorous)	Remendur
Electroloy	Rodar
Elinvar	Stainless Steel 202 <sup>2</sup>
Fenicoloy	Stainless Steel 302 <sup>2</sup>
Ferrites	Stainless Steel 303 <sup>2</sup>
Gridaloy M, P	Stainless Steel 304 <sup>2</sup>
Haynes Alloy #6	Stainless Steel 403 & 405
Invar	Stainless Steel 410 & 416
Iron	Stainless Steel 430 & 446
Kovar	Stainless Steel AISI 440C
Mesoloy	Supermalloy
Molypermallow	Ti 430
Monel K <sup>1</sup>	Vicalloy
Monel R	

<sup>1</sup>Based on a GSFC Materials Engineering Branch Technical Information Paper No. 128 entitled, "Minimizing Stray Magnetic Fields through Materials Selection".

<sup>2</sup>Non-magnetic (technically paramagnetic) in the annealed condition. If any of these alloys are cold worked then they will become magnetic. The alloy condition will be clearly indicated on the Material Certification that will accompany the purchase.

<sup>3</sup>Inconel alloys, 600, 625 and 718, are considered non-magnetic, but become magnetic at cryogenic temperatures.

### 7.3.2 Minimizing Stray Fields

Stray fields are due to uncompensated current loops or stray currents that result in permanent or variable magnetic moments. The AC and DC magnetic field or moment generated from the Front-End Electronics Assembly **shall** not exceed the following allocation in Table 7-2.

**Table 7-2: AC/DC Magnetic Field & Moment Allocation**

Unit	AC_limit (A-m <sup>2</sup> )	AC_dB_1M (nT)	DC_limit(A-m <sup>2</sup> )	DC_db_1m (nT)
Front-End Electronics Assembly	0.0152	3.03	0.209	41.7

#### 7.3.2.1 Minimizing Current Loops

Magnetic dipole moments are associated with the current loops and, if uncompensated, these can add up to large fields. The following guidelines may be used to minimize current loops:

- (1) Each positive wire that carries appreciable current ( $> 1$  mA) should be twisted with its return (see Section 0 for twisting details).
- (2) Where twisting is not possible (at connector pins, for example), positive and negative power lines should be routed to minimize the enclosed area between them. In connectors this is done by placing the positive and negative pins adjacent to each other..
- (3) On printed circuit boards, positive and negative power traces should be routed to minimize the enclosed area between them.

### **7.3.2.2 Compensating Current Loops**

It is not possible to completely eliminate current loops, and there are instances where the loop area cannot be minimized beyond a certain point. In these cases, the total field may be minimized by locating and orienting these loops in such a way as to generate opposing dipole moments that cancel each other.

### **7.3.2.3 Minimizing Stray Currents**

Stray fields can result from uncompensated conductors or currents flowing via “sneak paths” in the structure. The following techniques may be used to minimize stray currents:

- (1) Every wire carrying appreciable current ( $> 1$  mA) should have a return associated with it.
- (2) Stray currents associated with primary power can be eliminated by: (a) strict adherence to the single point grounding scheme for primary power, and (b) by isolating primary power from local signal and chassis grounds within components.
- (3) Interconnections between components should be carefully analyzed to determine all current paths.

## 8.0 DESIGN & CONSTRUCTION REQUIREMENTS

### 8.1 PARTS, MATERIALS & PROCESSES (PMP)

#### 8.1.1 EEE Parts

The *Front-End Electronics Assembly* contractor's Quality Assurance system for EEE parts **shall** be in accordance with the requirements in the SOW, 461-NAV-SOW-0021.

#### 8.1.2 Materials

The *Front-End Electronics Assembly* contractor's Quality Assurance system for materials **shall** be in accordance with the requirements in the SOW.

All parts should be passivated and mounting surfaces on *Front-End Electronics Assembly* **shall** be conductive as defined in Section 4.5.

Aluminum parts **shall** be finished with iridite per MIL-DTL-5541, Class 3.

Titanium surfaces **shall** be finished per AMS 2488.

Non-mounting surfaces **shall** be coated with a high emissivity coating (>0.7) such as black anodize per MIL-A-8625F Type II, Class 2.

#### 8.1.3 RESERVED

### 8.2 ELECTRICAL

#### 8.2.1 Test Sensors

Test sensors **shall** be designed for flight. Unless specified to be removed before flight, test sensors will not be removed prior to flight.

#### 8.2.2 Ground Strap Requirements

##### 8.2.2.1 Ground Straps, Length to Width Ration

All ground straps **shall** have a length-to-width ratio of less than 5 to 1.

##### 8.2.2.2 Ground Straps, Material

All ground straps **shall** be made of copper at least 1 mil thick, but still be flexible enough to attach to the spacecraft per the Mechanical ICD.

### 8.2.2.3 Ground Lug Contact Area

The grounding lug location on the component chassis or the tie points in contact with the ground strap **shall** have a minimum contact area of 80 mm<sup>2</sup>.

### 8.2.3 RESERVED

### 8.2.4 Mitigation of Internal Charging

Internal charging refers to the physical effect where high energy electrons deposit charge in a dielectric, if the charging rate is higher than the leakage rate eventually a point is reached where the dielectric discharges to the nearby structure.

#### 8.2.4.1 Mitigation Strategies for Internal Charging

There are a number of mitigation strategies possible to prevent charge build-up and subsequent arcing within components. Designers **shall** implement one, or more, of the following strategies:

- (1) Provide sufficient AL shielding (2.5mm for bulk dielectric or 1 mm for Tefzel cable).
- (2) Use low pass filters at either end of the cable that absorb the energy from the discharge without creating dangerous voltages.
- (3) Provide circuits at either end that have sufficiently low impedance that they are not harmed by the discharges
- (4) Provide circuits at either end that suppress transients (e.g. Transorbs). Note this method is undesirable because the Transorbs add unwanted failure mechanisms.

Note, that if the contractor uses strategies (2), (3) or (4), all affected circuit designs **shall** be analyzed to demonstrate compliance with the requirements, using a transient circuit analysis tool such as Pspice.

#### 8.2.4.2 Floating Conductors

Floating conductors, if present, **shall** have a bleed path of less than 10 MΩ to the component structure. This requirement is not applicable to small floating conductors (1 inch<sup>2</sup> or less) or short (1 inch or less) unterminated traces or wires that are inside of the components.

### 8.2.4.3 Dielectric Structures

#### 8.2.4.3.1 Bulk Resistivity

Dielectric structures with a bulk resistivity of greater than  $10^{12}$  ohm-cm **shall** be avoided.

#### 8.2.4.3.2 Charge Bleed-Off

All dielectric structures **shall** have a charge bleed path to the spacecraft interface, designed to route the discharge into the spacecraft structure in a controlled fashion.

### 8.3 SAFETY

### 8.4 ELECTROMAGNETIC COMPATIBILITY

The design of the components will be such that they are electromagnetically compatible with each other and with all the external environments in which they are expected to be operated. Specifically, the components will not: (a) generate electromagnetic interference that could adversely affect the operation and safety of each other, the launch vehicle, and other equipment present during ground operations; and (b) be susceptible to emissions that could adversely affect their operation and safety. These emissions may originate from each other, from the launch vehicle, or from other equipment present during ground operations.

The mode of transmission of electromagnetic interference may be conduction through wires or radiation through space. Electromagnetic compatibility requirements are designed to limit both conducted and radiated emissions and to minimize susceptibility to both types of emissions. These requirements can be grouped into four types:

- (1) Conducted emission requirements are designed to prevent excessive noise from being induced on the spacecraft power bus by components, subsystems, and instruments that are connected to the bus.
- (2) Conducted susceptibility requirements are designed to insure that any component, subsystem, or instrument connected to the spacecraft power bus is not unduly susceptible to noise expected to be present on the power bus.
- (3) Radiated emission requirements are designed to prevent excessive noise from being radiated by the observatory and its components.
- (4) Radiated susceptibility requirements are designed to ensure that spacecraft components, subsystems, or instruments are not unduly susceptible to radiated noise emanating from the observatory and other sources.

The following table summarizes the emission and susceptibility requirements.

**Table 8-1 Emission and Susceptibility Requirements**

Category	Description	MIL-STD-461C Identification	GEVS Paragraph Reference	Applicability
Conducted Emissions (CE)	DC Power Leads	CE01	2.5.2.1.a	Applicable for the primary power and return leads that supply power to a component. Not applicable for secondary power wires or signal wires except where noted in each test requirement section
		CE03	2.5.2.1.a&c	
		CMN (GEVS)	2.5.2.1.b	
		CE07	2.5.2.1.d	
Conducted Susceptibility (CS)	Power Lines	CS01	2.5.3.1.a	Applicable for the primary power and return leads that supply power to a component. Not applicable for primary power returns, secondary power wires, or signal wires.
	Power Lines	CS02	2.5.3.1.a	
	Power Line Transients	CS06	2.5.3.1.e	
Radiated Emissions (RE)	Magnetic Field	RE01	N/A	Applicable to all components.
	Electric Field	RE02	2.5.2.2.c	Applicable to all components.
Radiated Susceptibility (RS)	Electric Field	RS03	2.5.3.2.a	Applicable to all components.
RF Component Unique Tests	Antenna Port Emission	CE06	2.5.2.1.f	Only Applicable to RF Transmitters and Receivers
	Intermodulation	CS03	2.5.3.1.b	
	Rejection of Undesired Signals	CS04	2.5.3.1.c	
	Cross Modulation	CS05	2.5.3.1.d	

**8.4.1 RESERVED****8.4.2 RESERVED****8.4.3 Radiated Emissions**

Radiated emission requirements are designed to prevent excessive noise from being radiated by the spacecraft components.

**8.4.3.1 RE01 - Magnetic Field Emissions**

Component level magnetic field emissions **shall** not exceed the limits of Figure 8-1.

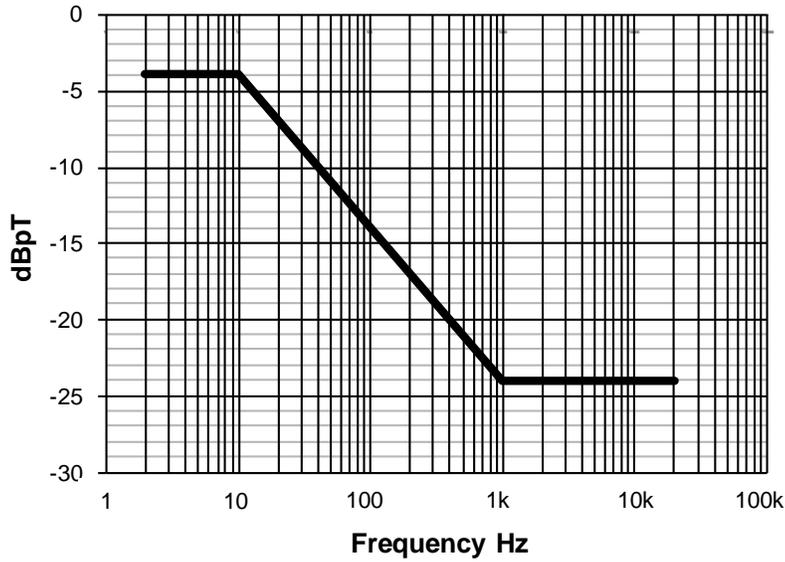


Figure 8-1 Component Level RE01 Radiated Magnetic Field Emission Limits

### 8.4.3.2 RE02 - Electric Field Emissions

Component level electric field emissions shall not exceed the limits of Figure 8-2.

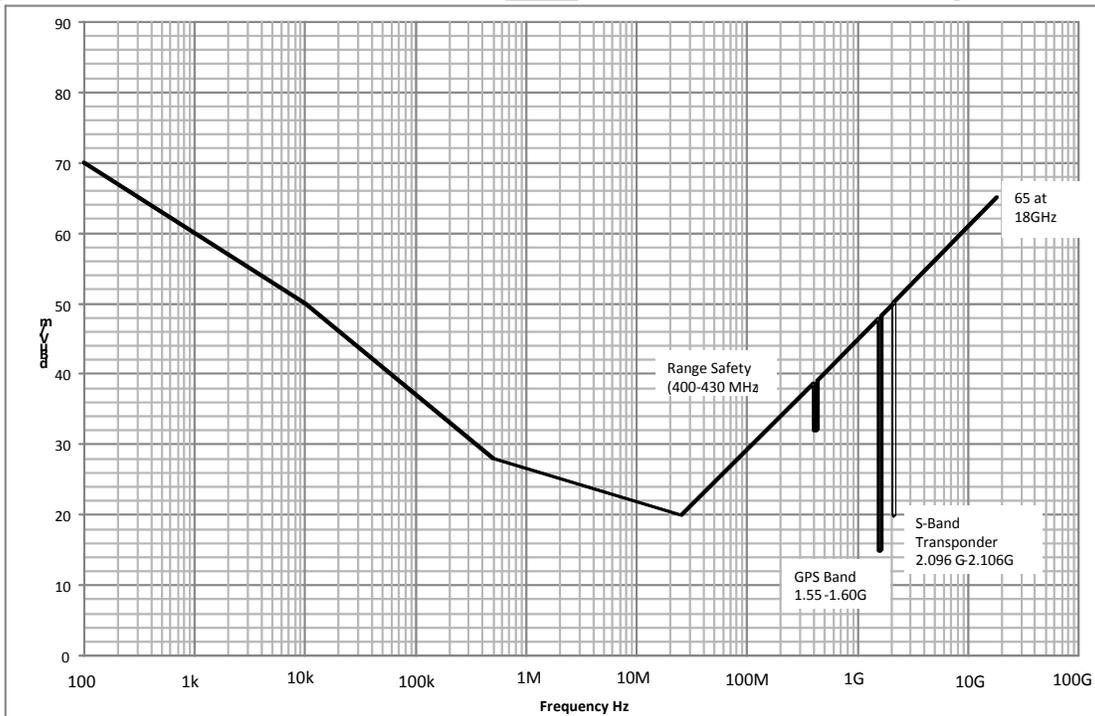


Figure 8-2 Component Level RE02 Radiated Electric Field Emission Limits

#### 8.4.4 Radiated Susceptibility

Radiated susceptibility requirements are designed to ensure that spacecraft components are not unduly susceptible to radiated noise emanating from the observatory and other sources.

##### 8.4.4.1 RS03 - Electric Field

The observatory and its components **shall** not malfunction or suffer degradation of performance when subjected to the radiated test signals that follow. Note that the GPS frequency band will be notched during RS03 test not to damage the amplifier.

20 V/m	14 kHz to 18 GHz
30 V/m	2281.9 $\pm$ 5 MHz (Observatory transmitter)
40 V/m	2211 $\pm$ 5 MHz (launch vehicle third stage telemetry transmitter)
40 V/m	5765 $\pm$ 5 MHz (launch vehicle second stage C-Band transponder)

#### 8.4.5 RF Component Unique Tests

In addition, the RF components **shall** meet the Antenna Port Emissions (CE06), Intermodulation (CS03), Spurious Signal (CS04) and Cross Modulation (CS06) requirements defined in GEVS.

### 8.5 IDENTIFICATION AND MARKING

Each unit **shall** be permanently marked with the part number and a unique sequential serial number in the area designated on the interface control drawing in a manner to be approved by the GSFC COTR.

All markings **shall** use alcohol proof ink.

### 8.6 WORKMANSHIP

#### 8.6.1 Workmanship Standards

The workmanship standards and processes outlined in the SOW **shall** be used.

#### 8.6.2 Connector

##### 8.6.2.1 GSE Cable Connectors

GSE cable connectors that mate with flight test connectors **shall** be flight-approved connectors.

##### 8.6.2.2 Prevention of Connector Mismatching

Connector mismatching prevention requirements are as identified in this section.

#### **8.6.2.2.1 Connector Uniqueness**

Physically adjacent connectors **shall** be of different sizes or of different sexes.

#### **8.6.2.2.2 Connector Facing**

Physically adjacent Rectangular “D” connectors **shall** not face the same way.

#### **8.6.2.2.3 Connector Keying**

Circular connectors **shall** be positively keyed.

#### **8.6.2.2.4 Accessibility**

The *Front-End Electronics Assembly* Spacecraft interface connectors should be spaced far enough apart to allow the mate and demate operations to be performed without a special tool. Any harness cable or connector should not touch any other adjacent connectors or harnesses.

#### **8.6.2.2.5 Connector Gender**

The connector half that sources power to another *Front-End Electronics Assembly* **shall** be female (socketed) to protect against inadvertent grounding prior to mating.

#### **8.6.2.3 Test Connectors**

Wherever possible, *Front-End Electronics Assembly* power **shall** not be applied or accessed at or through a test connector.

#### **8.6.2.4 Connector Identification**

Each harness connector **shall** be identified to facilitate mating by the use of a non-metallic band affixed to the cable which bears the reference designation of both the plug and the mating receptacle.

#### **8.6.2.5 Protection of Unused Test Connectors**

Test connectors **shall** be capped with flight-approved RF and static control covers when not in use.

#### **8.6.2.6 Connector Savers**

Connector savers **shall** be used during integration and test to minimize wear on connector contacts.

### 8.6.3 Safe/Arm Plugs

#### 8.6.3.1 Safe/Arm Plug Use

Safe and arm plugs should be incorporated in the cable or harness that control deployable actuators.

#### 8.6.3.2 Safe/Arm Plugs Connectors

Safe and arm plugs should use circular connectors in the cable or harness that control deployable actuators.

### 8.7 INTERCHANGEABILITY

Harness subassemblies and related components **shall** be directly interchangeable in form, fit, and function with other items of the same part number.

### 8.8 RELIABILITY

#### 8.8.1 Mission Life

The *Front-End Electronics Assembly* **shall** meet all performance specifications throughout 1 year of ground testing and 28 months of operation in space.

#### 8.8.2 Shelf Life

The *Front-End Electronics Assembly* **shall** not suffer any degradation in performance when stored for five (5) years either on the S/C or in bonded storage.

**9.0 LOGISTICS**

**9.1 RESERVED**

**9.2 RESERVED**

**9.3 RESERVED**

## 10.0 VERIFICATION REQUIREMENTS

The contractor **shall** conduct a verification program that demonstrates the hardware design is qualified and meets all requirements contained in this document. Per the SOW (461-NAV-SOW-0021), the contractor will provide a verification matrix defining the method of verification for each specific requirement of this document.

### 10.1 VERIFICATION METHODS

Verification methods include inspection, analysis, as well as environmental, functional, and performance testing, or a combination of these techniques.

#### 10.1.1 Inspection

Verification by inspection includes (but is not limited to) visual inspection, simple physical manipulation, gauging, measurement, and documentation examination.

#### 10.1.2 Analysis

Verification by analysis will be used to show design margins. Also, when the particular tests required for verification are impractical, risky, unacceptably long, or prohibitively expensive, analysis may be used instead of testing, as noted in the verification matrices.

Analysis, including simulations where applicable, will also be used to guarantee that the *Front-End Electronics Assembly* and its components will perform as expected under worst-case conditions.

#### 10.1.3 Test

Verification by test includes, but is not limited to, the evaluation of performance by use of special equipment or instrumentation, simulation techniques, and the application of established principles and procedures to determine compliance with requirements.

### 10.2 INSPECTION REQUIREMENTS

Verification by inspection **shall** be by one of these three methods: 1) visual inspection of the physical hardware; 2) a physical measurement of a property of the hardware, or; 3) a documentation search demonstrating hardware of an identical design has demonstrated fulfillment of a requirement.

#### 10.2.1 Visual Inspection

Visual inspection of the physical hardware **shall** be performed by a customer appointed qualified inspector certifying that the hardware has the properties/configuration specified in the requirement.

### 10.2.2 Physical Measurement

Physical measurement of hardware property (i.e. mass, dimensions, etc.) **shall** be performed by a customer appointed qualified inspector demonstrating the hardware meets specific requirement.

### 10.2.3 Documentation Search

Verification of requirements based on similarity **shall** include supporting rationale and documentation and **shall** be approved by the GSFC COTR

## 10.3 ANALYSIS REQUIREMENTS

Verification of performance or function through detailed analysis, using all applicable tools and techniques, is acceptable with GSFC COTR approval. Detailed descriptions of the minimum required analyses, as well as analysis requirements, are provided in the SOW.

## 10.4 TEST REQUIREMENTS

This section provides general test requirements on how testing is to be performed in the process of verifying that the deliverable item meets its requirements. Performance parameter measurements **shall** be taken to establish a baseline that can be used to assure that there are no data trends established in successive tests that indicate a degradation of performance trend within specification limits that could result in unacceptable performance in flight. Any requirement that exceeds previous qualification test data **shall** be presented to the MMS project as part of the verification planning process described in the SOW, for evaluation and a possible delta qualification test.

### 10.4.1 Definitions

The hardware definitions are reproduced here from Section 1.8 of GEVS (GSFC-STD-7000).

**Qualification or Prototype Hardware:** "Hardware of a new design; it is subject to a design qualification test program; it is not intended for flight." The purpose of the tests on this hardware is to prove that a new design meets one or more of its design requirements. Qualification testing is performed at maximum expected flight levels plus a margin. Test durations are typically longer than for acceptance tests.

**Protoflight Hardware:** "Flight hardware of a new design; it is subject to a qualification test program that combines elements of prototype and flight acceptance verification; that is, the application of design qualification test levels and flight acceptance test durations." The purpose of the test on this hardware is to prove that a new design meets one or more of its design requirements. Protoflight testing is performed at

maximum expected flight levels plus a margin. Test durations are typically the same as for acceptance tests.

**Follow-On (Acceptance) Hardware:** Flight hardware built in accordance with a design that has been qualified either as prototype or as protoflight hardware; follow-on hardware is subject to a flight acceptance test program.” The purpose of the test on this hardware is to prove that a particular flight unit has been manufactured properly. The design has already been proven during a qualification or protoflight test program. Acceptance testing is performed at maximum expected flight levels.

#### 10.4.2 Test Factors

The following test factors and durations, shown in Table 10-1, **shall** be used for prototype, protoflight, and follow-on flight hardware.

**Table 10-1 Test Factors and Durations**

Test	Prototype	Protoflight	Acceptance
Structural Loads Level Duration Centrifuge Sine Burst <sup>(1)</sup>	1.25 X Limit Load  1 Minute 5 Cycles Full Level	1.25 X Limit Load  30 Seconds 5 Cycles Full Level	Limit Load <sup>(2)</sup>  30 Seconds 5 Cycles Full Level
Acoustic Level Duration	Limit Level +3dB 2 Minutes	Limit Level +3dB 1 Minute	Limit Level 1 Minute
Random Vibration Level Duration	Limit Level +3dB 2 Minutes/Axis	Limit Level +3dB 1 Minute/Axis	Limit Level 1 Minute/Axis
Sine Vibration Level Sweep Rate <sup>(3)</sup>	1.25 X Limit Level 2 Octaves/Minute/Axis	1.25 X Limit Level 4 Octaves/Minute/Axis	Limit Level 4 Octaves/Minute/Axis
Shock Actual Device Simulated	2 Actuations 1.4 X Limit Level 2 Actuations/Axis	2 Actuations 1.4 X Limit Level 1 Actuations/Axis	1 Actuation Limit Level 1 Actuation/Axis

(1) Sine burst testing **shall** be done a frequency sufficiently below primary resonance as to ensure rigid body motion.

(2) All composite structures must be tested to 1.25 x limit loads. All beryllium structures must be tested to 1.4 x limit loads.

(3) Unless otherwise specified these sine sweep rates **shall** apply.

#### 10.4.3 Test Tolerances

Tolerances for the various mechanical test parameters are given in Table 10-2.

Table 10-2 Test Tolerances

Test	Test Parameter	Tolerance	
Acoustics	Overall Level:	≤ 1dB	
	1/3 Octave Band Frequency:		
	f ≤ 40 Hz	+ 3, - 6 dB	
	40 < f < 3150 Hz	± 3 dB	
	f ≥ 3150 Hz	+ 3, - 6 dB	
Temperature		± 2 °C	
Humidity		± 5% RH	
Loads	Steady-State (Acceleration):	± 5%	
	Static:	± 5%	
Mass Properties	Weight:	± 0.2%	
	Center of Gravity:	± 2 mm	
	Moments of Inertia	± 1 %	
	Products of Inertia	± 5 %	
Mechanical Shock	Response Spectrum:	+ 25%, - 10%	
	Time History:	± 10%	
Pressure	>1.3 x 10 <sup>4</sup> Pa (> 100 mm Hg):	± 5%	
	1.3 x 10 <sup>4</sup> to 1.3 x 10 <sup>2</sup> Pa (100 mm Hg to 1 mm Hg):	± 10%	
	1.3 x 10 <sup>2</sup> to 1.3 x 10 <sup>1</sup> Pa (1 mm Hg to 1 micron):	± 25%	
	< 1.3 x 10 <sup>1</sup> Pa (< 1 micron):	± 80%	
Vibration	Sinusoidal:	Amplitude	± 10%
		Frequency	± 2%
	Random:	RMS Level	± 10%
		Accel. Spectral Density	± 3 dB

#### 10.4.4 Test Restrictions

##### 10.4.4.1 Failure During Tests

When a failure (non-conformance or trend indicating that an out-of-spec condition will result) occurs, determination will be made as to the feasibility and value of continuing the test to its specified conclusion. The test **shall** be stopped if equipment fails during testing in cases where this failure will result in damage to the equipment. Otherwise, the test **shall** be completed to obtain as much information as possible. If corrective action is taken, the test will be repeated to the extent necessary to demonstrate that the test item's performance is satisfactory. If corrective action taken as a result of failure affects the validity of previously completed tests (e.g., redesign of a component), prior tests will be repeated.

If during a test sequence, a test item is operated in excess of design life and wears out or becomes unsuitable for further testing from causes other than deficiencies, a spare will be substituted, and previously completed tests will be repeated to the extent necessary.

No replacement, adjustment, maintenance, or repairs are authorized during testing. This requirement does not prevent the replacement or adjustment of equipment that has exceeded its design operating life during tests, provided that after such replacement,

the equipment is tested as necessary to assure its proper operation. A complete record of any exceptions taken to this requirement **shall** be included in the test report.

#### 10.4.4.2 Modification of Hardware

Once the formal acceptance test has started, cleaning, adjustment, or modification of test hardware **shall** not be permitted.

#### 10.4.4.3 External Adjustment

The *Front-End Electronics Assembly* **shall** be designed so that no external adjustments are required after start of acceptance or qualification testing.

#### 10.4.4.4 Re-Test Requirements

If any event, including test failure, requires that a *Front-End Electronics Assembly* be disassembled and reassembled, then all tests performed prior to the event must be considered for repeat. If the unit has multiple copies of the same build, then all units must be examined to determine if the problem is common. If all copies require disassembly for repair, then each must receive the same test sequence.

### 10.5 **REQUIRED TESTS**

The following tests are required for each *Front-End Electronics Assembly* to provide assurance that the *Front-End Electronics Assembly* meets its all of its requirements. Each test or demonstration is described below:

- Performance Testing
- Mass Properties
- Static Load/Strength
- Sine Sweep Survey
- Sine Vibration
- Random Vibration
- Acoustics (on selected components)
- Shock (on selected components)
- Electromagnetic Compatibility
- Magnetism
- Thermal Bake-Out
- Thermal Vacuum
- Thermal Cycling

## 10.5.1 Performance Tests

### 10.5.1.1 Comprehensive Performance Test

The Comprehensive Performance Test (CPT) will be used to verify full compliance of each flight unit to all of its performance requirements, within the limitations of the environment and facilities. The CPT will be designed to verify unit performance in all modes and configurations and under varying input/output conditions.

### 10.5.1.2 Functional Test

The Functional Test (FT), also known as a Limited Performance Test (LPT), is a subset of the Performance Test and is designed to verify functionality of the flight unit under nominal input/output conditions. The FT will be used to verify unit operation when it is not practical to use the CPT. Typically, it is used during and after certain environmental tests to demonstrate that the functional capability of the component has not been degraded due to environmental exposure, handling, and transportation. It is also commonly used during some of the hot and cold plateaus during thermal vacuum testing.

### 10.5.1.3 Abbreviated Functional Test

An Abbreviated Functional Test (AFT) may be used when it is necessary to monitor the performance of the flight unit over a very short period of time. The AFT is typically used when a unit is being subjected to vibration testing.

### 10.5.1.4 RESERVED

## 10.5.2 Mass Properties Measurement

Measurement of the weight and center of gravity of each flight hardware component will be made to show compliance with requirements and to provide accurate data for the observatory mass properties control program. Center of gravity at the component level will be referenced to the component to spacecraft mounting interface.

## 10.5.3 Static Loads/Strength Test

Strength testing is used to verify the component strength and structural integrity (beryllium and composite materials cannot be qualified by analysis alone), and it can be done using a variety of techniques, such as sine burst, static pull, or centrifuge testing.

Structural design loads **shall** be applied to prototype or protoflight hardware. There is no requirement to strength test flight hardware that has already been strength tested through a prototype or protoflight program (ie, there is no “acceptance level” strength test requirement for flight hardware).

No permanent deformation may occur as a result of the loads test, and all applicable alignment requirements must be met following the test. Units that require alignment will have an alignment check following loads testing.

The *Front-End Electronics Assembly* **shall** be powered during static loads tests if the item will be powered during launch. A performance test **shall** be conducted after the loads test to verify that no damage occurred due to the loads test. A functional test **shall** be performed before the start of testing and after a test in each axis if sine burst is used.

#### 10.5.3.1 Sine Burst

If sine burst test is selected, the test will be performed in each of three orthogonal component axes. A simple Sine Burst test following the random vibration test in each axis is a convenient method to conduct a structural loads test. Test frequency will be less than one-third of the resonant frequency of the component to avoid dynamic amplification during test. This test applies a ramped sine input at a sufficiently low frequency such that the test item moves as a rigid body. The test will be conducted in a stepwise manner starting with lower level sine-bursts that are fractions of the full load. An analysis is required to show that a base drive Sine Burst test will not cause over-test or under-test in some areas of the structure. The number of cycles at maximum level will be at least 5.

#### 10.5.3.2 Static Pull

Static pull tests are another method to perform loads testing and can be applied at flight interfaces in a static test facility. The loads can be applied either as *Front-End Electronics Assembly* loads applied simultaneously, or the single resultant vector load can be applied to the test point. Strain gages are generally positioned around the test point to verify deflection predictions from the analytical model. The Test Duration **shall** be at least 30 seconds.

#### 10.5.4 Sine Sweep Survey

The Sine Sweep **shall** be conducted on each *Front-End Electronics Assembly* before and after vibration testing in each axis. A low-level sine sweep is used to determine the modal signature of the flight item to verify compliance with fundamental frequency requirements, and to verify no change in structural integrity from testing. Test parameters will be as follows:

- Frequency: 5 - 2000 Hz
- Acceleration: 0.25 g
- Sweep Rate: 2 octaves/minute

This test will be performed immediately preceding the sine/random vibration tests and will be repeated after the sine/random vibration tests to verify that the modal signature of the unit under test (first resonant frequency) is within 5% of the pre-test frequency. In

this case, the unit has passed and the test can continue. If the post-test frequencies are between 5% and 10% of the pre-test frequencies, the cause of the shift should be investigated (test bolt torques, etc.) before determining whether failure has occurred or success has been achieved and whether the test can continue. A shift of greater than 10% indicates failure, and the test should be terminated, and the failure documented. In either case when the shift is greater than 5%, NASA/GSFC **shall** be notified.

Frequencies **shall** be verified and reported up to 200 Hz. Any component which fails to meet the specified fundamental frequency must supply a finite element model, correlated to modal survey test results up to 50 Hz, to be used in coupled loads analyses.

### 10.5.5 Sine Vibration

The *Front-End Electronics Assembly* **shall** be subjected to swept sine vibration testing to the appropriate levels and durations shown in the mechanical requirements section.

Sine vibration test is intended to verify workmanship quality and to simulate launch vehicle loading conditions. The test will consist of a low frequency sine transient or sustained sine environment that would be present in launch by minimum modal frequency in each of three mutually perpendicular axes, one of which is normal to the mounting surface.

For the sine vibration tests, the unit under test will be attached to the vibration table using the same configuration, attachment points, preloads, and attachment hardware that will be used during launch and flight. Cross-axis responses of the fixture will be monitored to preclude unrealistic levels. During the test, the test input level will be reduced (notched) at critical frequencies, if required, to limit the vibration loads and/or acceleration responses to 1.25 times design limit levels. During the vibration test, the flight unit will be powered and critical signals monitored and recorded using recording instruments that have a response equal to or greater than the highest frequency of vibration (this requirement applies only to those units that are expected to be powered during launch). A functional test **shall** be performed before the start of testing and after a test in each axis.

### 10.5.6 Random Vibration

The *Front-End Electronics Assembly* **shall** be subjected to a random vibration test in each of three orthogonal axes of the unit under test, one axis being perpendicular to the mounting surface to the appropriate levels and durations shown in the environmental requirements section. Random vibration test is intended to demonstrate workmanship quality and to simulate launch vehicle aerodynamic environmental levels. During the test, the test input level will be reduced (notched) at critical frequencies, if required, to limit the random vibration loads and/or acceleration responses to 1.25 times design limit

levels. Notching will be limited to -12 dB of the original input and to a bandwidth of less than 100 Hz (notching beyond these limits will require MMS project approval).

For the random vibration test, the unit under test will be attached to the vibration table using the same configuration, attachment points, preloads, and attachment hardware that will be used during launch and flight. Prior to the test, a survey of the test fixture/exciter combination will be performed to evaluate the fixture dynamics and the proposed choice of control accelerometers. Cross-axis responses of the fixture will be monitored during the test to preclude unrealistic levels.

During the vibration test, the flight unit will be powered and critical signals monitored and recorded using recording instruments that have a response equal to or greater than the highest frequency of vibration (this requirement applies only to those units that are expected to be powered during launch). A functional test **shall** be performed before the start of testing and after a test in each axis.

#### 10.5.7 Acoustic Test

The acoustic test will be conducted in an area large enough to maintain a uniform sound field at all points surrounding the unit under test. The sound pressure levels at various frequencies will be as specified in the Environmental Requirements section. During acoustics tests, the flight unit will be powered and critical signals monitored and recorded using recording instruments that have a response equal to or greater than the highest acoustic frequency (this requirement applies only to those units that are expected to be powered during launch). A functional test **shall** be performed before the start of testing and after the acoustic test.

#### 10.5.8 RESERVED

#### 10.5.9 Shock

Shock test is designed to verify that flight hardware will survive expected shock events such as observatory separation, boom deployment, etc.

The *Front-End Electronics Assembly* **shall** be assessed as to whether it is shock sensitive or not. Items that are more likely to be shock sensitive include very brittle materials (e.g., glass, ceramics), wire bonds, sensors, transducers, and filters.

If the item is deemed shock sensitive or deemed to contain shock-sensitive parts, then the hardware must be qualified for the shock environment by demonstrating a 3dB margin against the shock response spectrum given in Table 6-5. Previous shock testing may be used to demonstrate qualification. If a positive margin can be demonstrated, then the item is considered qualified for shock based on heritage.

If no data exist or a 3dB margin cannot be demonstrated based on prior testing, then a component level shock test is required. Shock testing may be performed at the sub-component or part level so as to limit the test risk to the flight hardware.

If the *Front-End Electronics Assembly* is not deemed shock sensitive, then qualification for the shock environment is not required, and the shock testing can be deferred to the level of assembly that allows for actuation of the actual shock-producing device.

### 10.5.10 Thermal Bake-out

The *Front-End Electronics Assembly* **shall** be baked-out prior to delivery to GSFC to reduce outgassing of contaminants to meet the requirements on Section 7.1.2.2.2. The rate measured at the QCM **shall** be adjusted to account for chamber geometry, presence of cold sinks, chamber pumping speed, view factors of the QCM, and any other factors necessary to assure an accurate measurement of the total outgassing per unit time per Kg mass of the unit under test.

### 10.5.11 Thermal Vacuum Test

#### 10.5.11.1 Thermal Vacuum Test Parameters

Thermal vacuum testing **shall** be conducted in accordance with the requirements of Table 10-3.

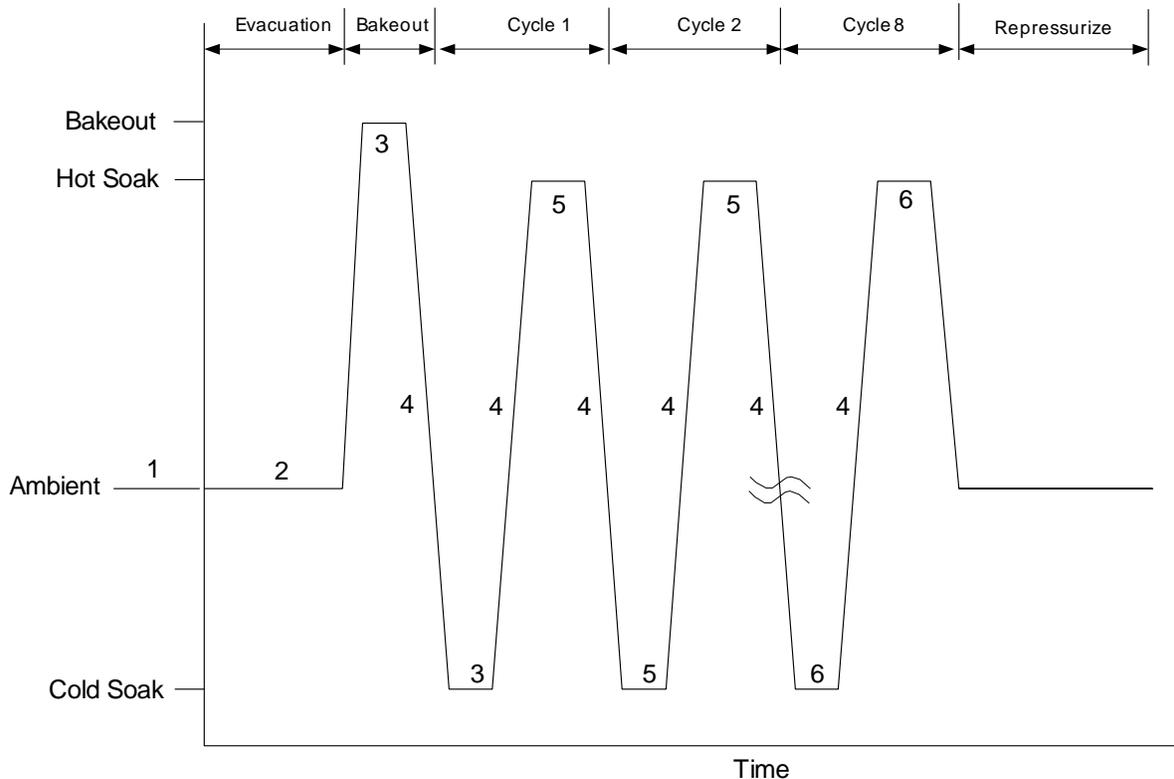
**Table 10-3 Thermal Vacuum Test Parameters**

Parameter	Component Level
Chamber Pressure After Evacuation	$< 5 \times 10^{-5}$ Torr
Number of Cycles	8
Acceptance Temperature Limits (beyond operational limits)	5 °C
Proto-flight Temperature Limits (beyond operational limits)	10 °C
Temperature Rate of Change	2 – 4 °C per minute
Minimum Dwell Time (at cold and hot plateaus)	4 hrs
Cold/Hot Turn On of Components (at cold and hot plateaus)	Yes
Total Number of Comprehensive Performance Tests (at least one each at cold and hot plateaus)	$\geq 2$

#### 10.5.11.2 Thermal Vacuum Test Profile

During Thermal Vacuum testing, the *Front-End Electronics Assembly* **shall** be in flight configuration, with the possible exception that items that do not involve mechanisms may remove their thermal blankets to speed the transition times between temperature extremes.

The *Front-End Electronics Assembly* **shall** apply the Thermal Vacuum Test profile shown in Figure 10-1. Note that there are to be eight cycles.



- (1) A CPT will be performed prior to the start of chamber evacuation.
- (2) The component will be powered and critical parameters monitored using the AFT during chamber evacuation. For RF components that are expected to be powered during launch, the absence of corona or multipaction effects will be verified.
- (3) Cold-start and hot-start capability will be demonstrated by performing CPTs at first cold and hot plateaus.
- (4) During the transition between temperature extremes, the component will remain powered and its performance will be monitored and recorded using the AFT.
- (5) LPTs will be performed after a soak period at the high/low temperature plateaus during Cycles 2-7.
- (6) Cold-start and hot-start capability will be demonstrated again at the eighth cold and hot plateaus.

**Figure 10-1 Thermal Vacuum Profile**

### 10.5.12 RESERVED

### 10.5.13 Thermal Cycling Testing

Some components (such as solar panels) may require life-cycle thermal testing to qualify the design. Since it is not practical to perform very large number cycles in vacuum, additional thermal cycling at ambient pressure may be used on qualification units to increase the total number of cycles (prior to ambient-pressure thermal cycling, the units are still required to undergo thermal vacuum cycling as called out above).

Performance tests will be performed periodically during these cycles to detect problems early.

#### **10.5.14 RESERVED**

#### **10.5.15 EMI/EMC Tests**

EMC tests comprise emissions and susceptibility tests. Emissions tests are intended to verify that the flight unit does not generate either conducted or radiated interference that could hinder the operation of other components, and susceptibility tests are intended to verify that the flight unit will operate properly when subjected to conducted or radiated interference from other sources. It is encouraged to perform these EMI tests as early as possible in the development.

All tests **shall** be performed with the *Front-End Electronics Assembly* in its most sensitive mode for susceptibility testing and in its most noisy mode as appropriate for the EMI emission test.

##### **10.5.15.1 Radiated Emissions Tests**

The radiated emissions tests **shall** be performed on the first flight units only.

##### **10.5.15.2 Radiated Susceptibility Tests**

The radiated susceptibility tests **shall** be performed on the first flight units only.

#### **10.5.16 Electrostatic Cleanliness Verification**

Electrostatic cleanliness verification is needed to ensure that the surfaces of external components are within their respective allocated surface resistivity requirements.

All exposed surfaces of the *Front-End Electronics Assembly* **shall** be tested for surface conductivity and charge bleed-path to the observatory structure.

#### **10.5.17 Magnetic Tests**

The magnetic tests are needed to identify magnetic parts and to ensure that the *Front-End Electronics Assembly* is within its respective allocated magnetic field requirements. Magnetic acceptance testing is required to be performed just prior to delivery of the component or subsystem, but it is recommended that early tests be performed to detect potential problems early. Magnetics testing will be performed by NASA/GSFC personnel as specified in the SOW, 461-NAV-SOW-0021.

**APPENDIX A ABBREVIATIONS AND ACRONYMS**

<b>Abbreviation/ Acronym</b>	<b>Definition</b>
AC	Alternating Current
AFT	Abbreviated Functional Test
Al	Aluminum
CCB	Configuration Control Board
CCR	Configuration Change Request
CE	Conducted Emissions
CG	Center of Gravity
CM	Configuration Management
CMO	Configuration Management Office
CMOS	Complementary Metal Oxide Semiconductor
COTR	Contracting Officer's Technical Representative
CPT	Comprehensive Performance Test
CS	Conducted Susceptibility
CVCM	Collected Volatile Condensable Mass
DA	Double Amplitude
DC	Direct Current
DDD	Displacement Damage Dose
DILS	Deliverable Items List and Schedule
EED	ElectroExplosive Actuators
EEE	Electrical, Electronic, and Electromechanical
ELDR	Enhanced Low Dose Rate
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EOL	End of Life
ESD	Electrostatic Discharge
ETU	Engineering Test Unit
FEA	Front-End Electronics Assembly
FS	Factor of Safety
FT	Functional Test
GeBK	Germanium Black Kapton
GPS	Global Positioning System
GSE	Ground Support Equipment
GSFC	Goddard Space Flight Center
ICD	Interface Control Drawing
I&T	Integration and Test
ITO	Indium Tin Oxide
LET	Linear Energy Transfer
LPT	Limited Performance Test
LVDS	Low Voltage Differential Signal

Abbreviation/ Acronym	Definition
MBU	Multi Bit Upset
MLI	Multi-Layer Insulation
MMS	Magnetospheric Multiscale
Mohms	Megaohms
MOP	Maximum Operating Pressure
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MS	Margin of Safety
NASA	National Aeronautics and Space Administration
NEA	Non-Explosive Actuators
NIEL	Non-Ionizing Energy Loss
OSR	Optical Solar Reflector
PDL	Product Design Lead
QCM	Quartz Crystal Monitor
RE	Radiated Emissions
RF	Radio Frequency
RS	Radiated Susceptibility
SC	Spacecraft
SCoRe	Signature Controlled Request
SEB	Single Event Burnout
SEGR	Single Event Gate Rupture
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEL	Single Event Latchup
SEM	Scanning Electron Microscope
SEU	Single Event Upset
SHE	Single Hard Error
SOW	Statement of Work
SPL	Sound Pressure Level
STP	Solar Terrestrial Probe
TBD	To Be Defined
TBR	To Be Reviewed
TID	Total Ionizing Dose
TML	Total Mass Loss
UUT	Unit Under Test
VDA	Vapor Deposited Aluminum
VDC	Voltage, Direct Current